

## DWA TECHNIQUE TO IMPROVE DAC OF SIGMA-DELTA FRACTIONAL-N FREQUENCY SYNTHESIZER FOR WiMAX

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### Abstract

A first order of DWA (Data Weighted Averaging) algorithm with third order sigma-delta modulator is proposed for application in sigma-delta fractional-N frequency synthesizer for WiMAX. In addition, this paper discusses the impact of mismatch between Digital-to-Analog convertor (DAC) unit elements. The simulation results show the effectiveness of the DWA technique in reduction of spurs, also DWA technique proves its ability to solve DAC unit elements mismatch. The fractional spur noise is converted into a broadband. Quantization noise with DWA is improved by – 10 dB if the element mismatch 0.01 and – 5 dB if the element mismatch 0.08 with 8 bit PFD/DAC. Matlab (V.7) program is used for simulation.

**Key words:** WiMAX, Frequency synthesizer, DAC mismatch, DWA technique.

### Introduction

WiMAX (Worldwide Interoperability for Microwave Access) also referred to as IEEE 802.16, is a broadband technology that provides wireless services connectivity to fixed, nomadic, portable, and mobile users [1]. However the present standards, such as wireless fidelity (Wi-Fi), fail to provide sufficient high data rate, long range and low deployments costs, while WiMAX overcomes the above problems [2]. However, common to all wireless communication system is the frequency synthesizer (FS). The frequency synthesizer is the heart and the most critical part of these systems [3]. The number of frequencies generated, spurious levels and the switching rate are the main quantities that determine system capabilities of the synthesizer itself. Recently, synthesizers used sigma-delta modulator. This delta-sigma modulator uses oversampling and noise shaping to reduce the phase noise [4,5]. The quantization noise-bandwidth tradeoff associated with  $\Sigma\Delta$  fractional-N synthesis can be removed if quantization noise can be reduced. Fig.(1) shows a block diagram of a  $\Sigma\Delta$  fractional-N PLL frequency synthesizer. The key advantage of this proposed method is that the circuitry that injects quantization noise into the loop (the PFD and charge-pump) is combined with the cancellation signal by DAC to create an inherent gain match between the two signals. The resulting mismatch

compensated PFD/DAC synthesizer is capable of dramatically reducing quantization induced phase noise [6, 7], as shown in Fig. (2). The PFD/DAC block which is a combination of PFD and DAC in one single element is used to overcome non-idealities between them, as shown in Fig. (1). The main source of mismatch in the charge-pump portion of the PFD/DAC is the mismatch between the DAC unit elements, for this reason, a DAC mismatch compensation block is used [6], as shown in Fig. (2). Thermometer decoder and data weight averaging (DWA) circuit, are used to shape mismatch noise to high frequencies [8].

### DWA Algorithm

Mismatch in the DAC unit elements causes distortion in the signal band which reduces the obtained signal to noise plus distortion ratio (SNDR). To solve this problem, DAC uses dynamic element matching (DEM) techniques. The functional principle of all DEM techniques is to transfer distortion that occurs due to the fixed step-size errors into a noise signal that is spread over the whole frequency band up to half of the sampling frequency, then shaping to high frequency [9]. The components of the quantization noise and the DAC noise outside of the signal band in Fig. (3a) will be removed by the filter but much of the DAC noise will be in band. Using noise-shaping DEM techniques results in DAC noise that pushes DAC noise outside the signal

band as illustrated in Fig. (3b). There are several DEM techniques which have been published (Barrel-Shift, Individual Level Averaging (ILA), and Data Weighted Averaging (DWA) algorithms) [9]. Data Weighted Averaging DWA [9,10] is the most popular DEM technique, because of its simple implementation and efficiency. The basic DWA for a 4-bit DAC [6,8] is illustrated in Fig.(4). Sigma-delta modulator output codes denoted as  $y(n)$ , range from one to four unit ( $U_1, U_2, U_3, U_4$ ), as shown in Fig. (4). The counter is used to create pointer ( $ptr(n)$ ) that shows the point of first unused unit element,  $IM(ptr(n))$ , referred to as integral mismatch, is the accumulation of the element mismatch error. The code is converted to thermometer code ( $2^B - 1$ ), and a logarithmic shifter is used to move the origin of the thermometer code to the new position. The algorithm cycles through the DAC elements by sequentially selecting the elements based are upon the input data, as shown in Fig. (5). Mathematically, DAC mismatch noise ( $N_{DAC}$ ) can be defined as a function of the  $IM(ptr(n))$  in Z-domain [8]:

$$N_{dac}(z) = (1 - z^{-1}) \times IM(ptr(z)) \dots\dots\dots (1)$$

Where  $(1 - z^{-1})$  is a first order high-pass filtered of the integral mismatch error generated and

$$IM(ptr(n)) = \sum_{i=0}^{ptr(n)-1} (U_i - U_{mean}) / (U_{mean}) \dots\dots\dots (2)$$

$$= \sum_{i=0}^{ptr-1} e_i \dots\dots\dots (3)$$

Where  $U_{mean}$  is the average value of the DAC unit elements,  $U_{mean} = \frac{1}{N} \sum_{i=0}^{N-1} U_i$ ,  $U_i$  is the  $i$ th DAC unit element value,  $e_i$  is the DAC mismatch error of  $i$ th DAC unit element, and  $N$  is the number of total DAC unit.

The flow chart of DWA algorithm is shown in Fig. (6).

**Simulation Results**

The PFD/DAC is composed of  $2^B$  unit elements, where B is the number of bits in the PFD/DAC. Mismatch between the unit

elements results in a gain mismatch between the quantization noise signal and cancellation signal. In order to match the unit elements, the data weighted averaging (DWA) algorithm is used. Without DWA enabled, the unit element mismatch leads to a large amount of fractional spur feed-through. Figs. (7) and (8) present the results of simulation for several values of DAC unit element mismatch ( $\sigma$ ) with different multi-bit PFD/DAC. These simulation results show the impact of increase in mismatch value ( $\sigma=0.01$  and  $\sigma=0.08$ ) between DAC unit elements on overall performance of PLL, which causes increase in the phase noise and large amount of fractional spur feed-through at the output spectrum of PLL. The minimum value of  $\sigma$  result of low spur appears at the output, as shown in Fig. (7). As the mismatch value ( $\sigma$ ), between DAC unit elements, is increased, more significant spurs result, and adversely affect synthesizer performance, as shown in Fig. (8). In order to evaluate the impact of increase in DAC unit elements of current sources mismatch on PFD/DAC performance, a suite of simulations was run with the PFD/DAC resolution set to 12 bit, as shown in Fig. (9). Simulation results show that the high spurs appear at the output of PFD/DAC block, and result in high contents of spurs.

**Conclusions**

Mismatch between DAC elements is studied and shows that the spurious levels increase with increasing the mismatch between DAC elements. It was found that DWA algorithm proves its ability to solve this problem. The net improvement in quantization noise is obtained (- 10 dB) if  $\sigma = 0.01$  and (-5 dB) if  $\sigma = 0.08$  with 8 bit. However, the quantization noise with DWA is improved by (- 8 dB) if  $\sigma = 0.01$  and (- 3 dB) if  $\sigma = 0.08$  with 12 bit PFD/DAC. Therefore DWA technique is proposed to be used in sigma-delta fractional-N frequency synthesizer for WiMAX system.

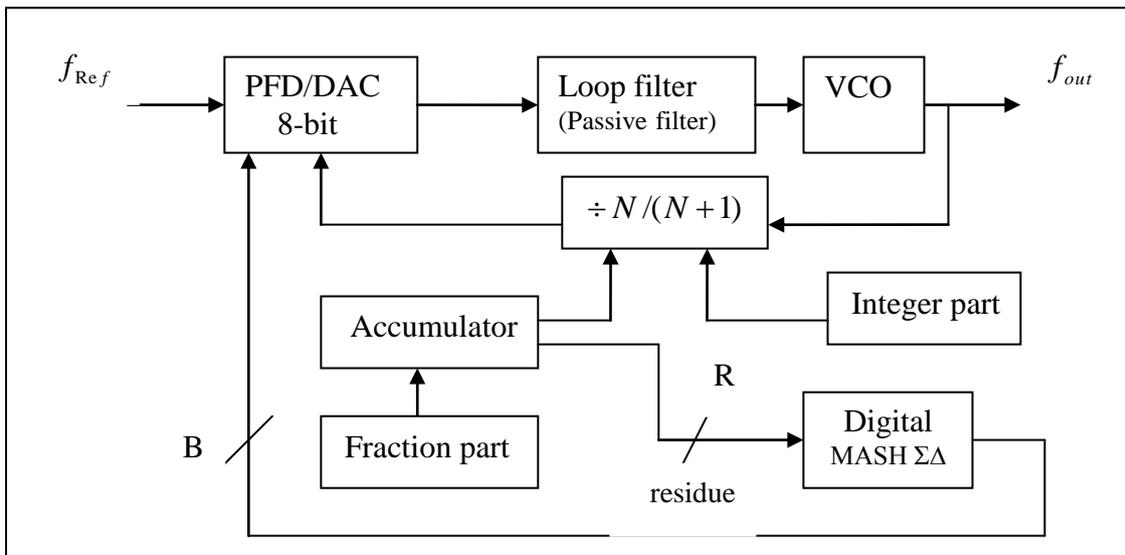


Fig. (1) : Block diagram of PFD/DAC frequency synthesizer.

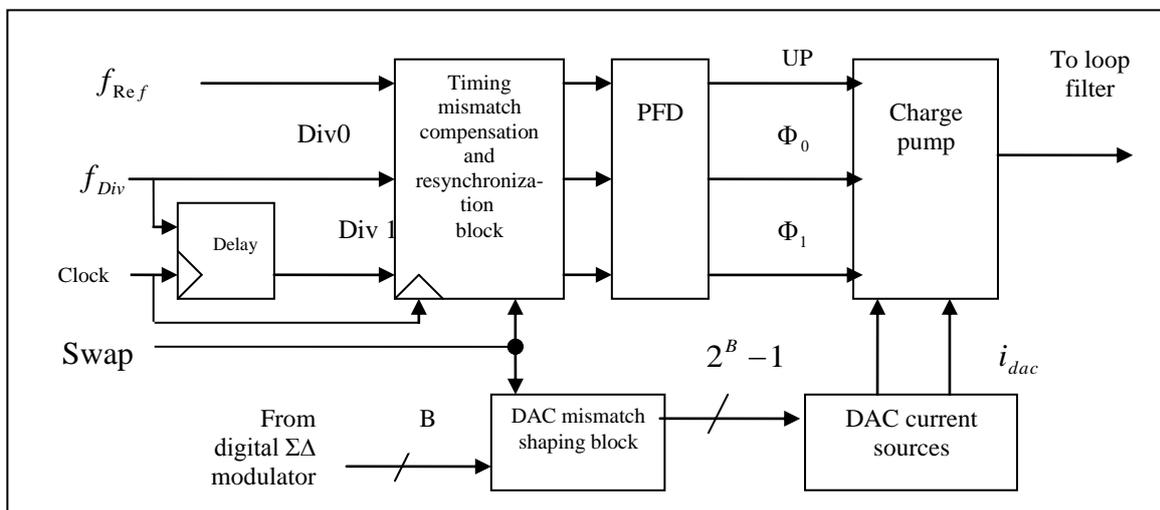


Fig. (2) : PFD/DAC block diagram.

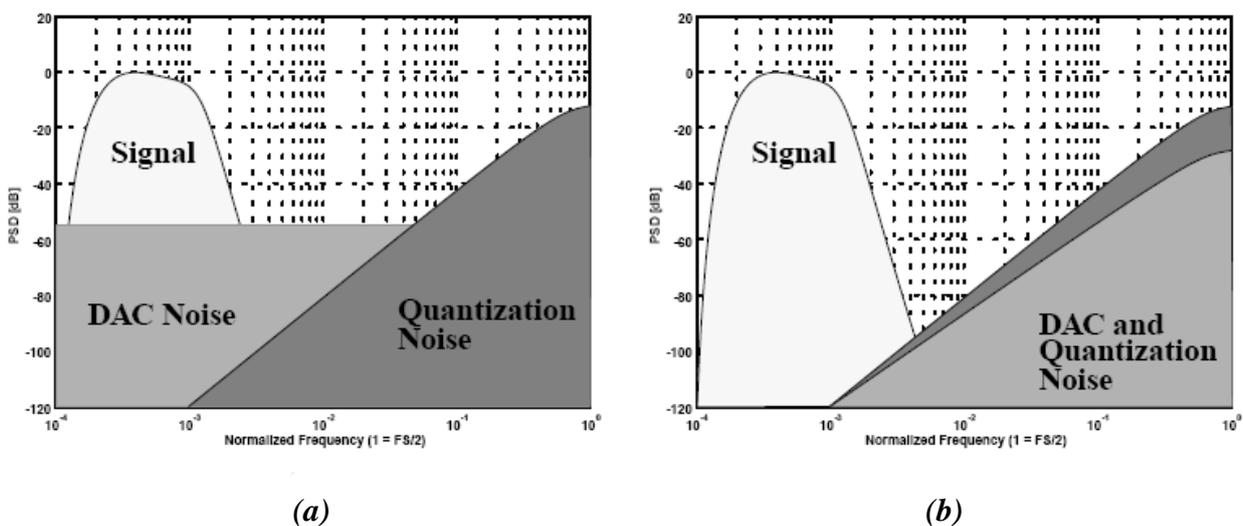
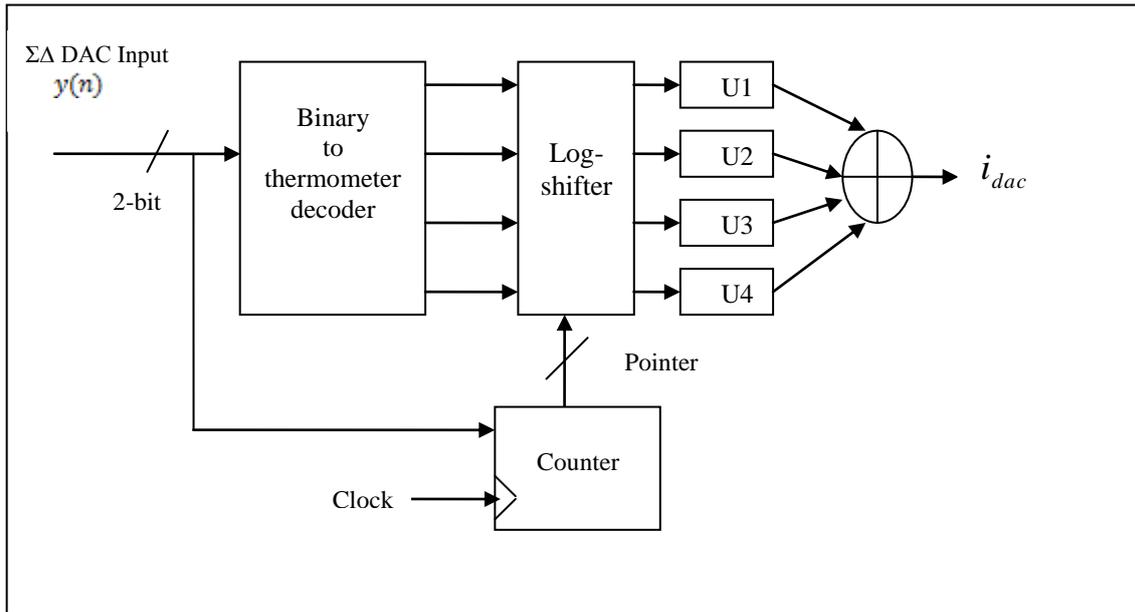
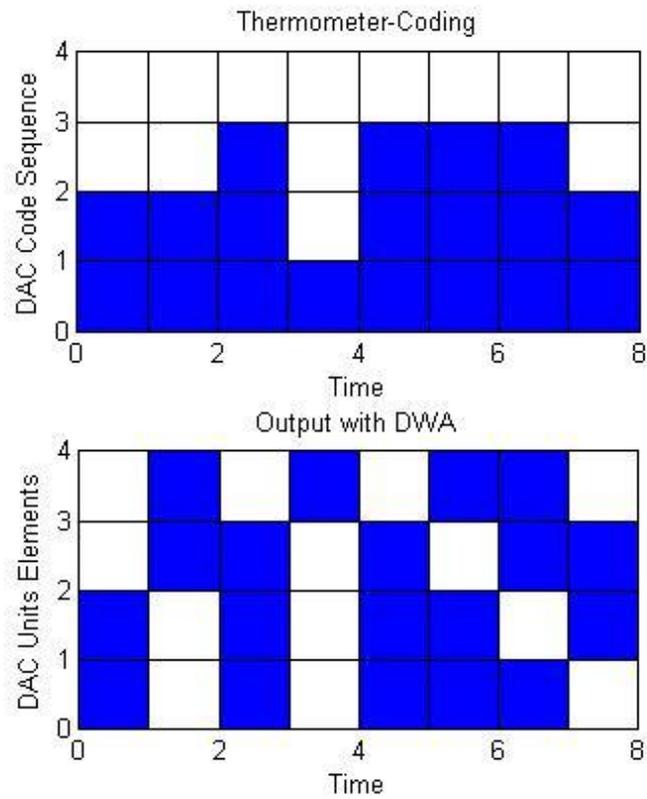


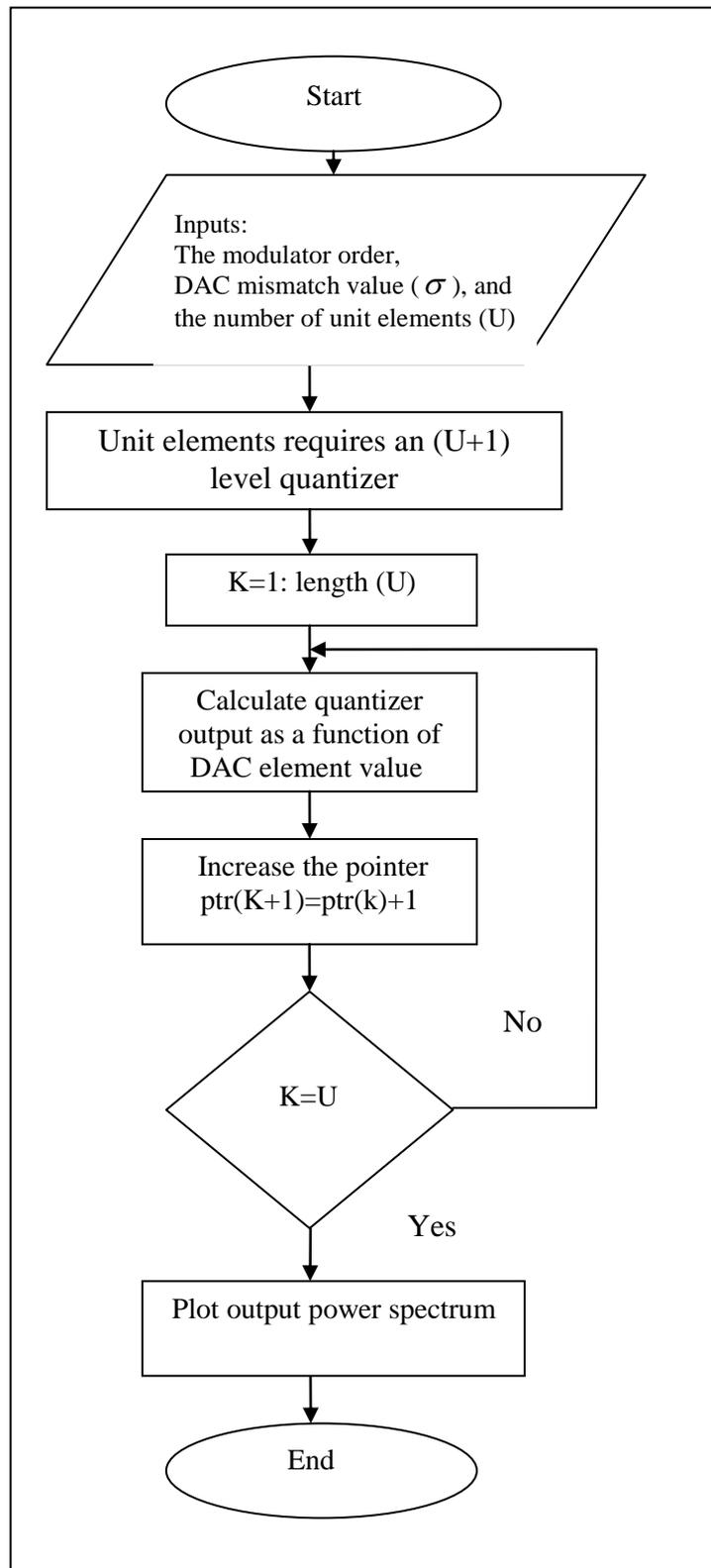
Fig. (3): Typical power spectral densities at the output of the DAC  
 (a) without DEM (b) with DEM algorithm.



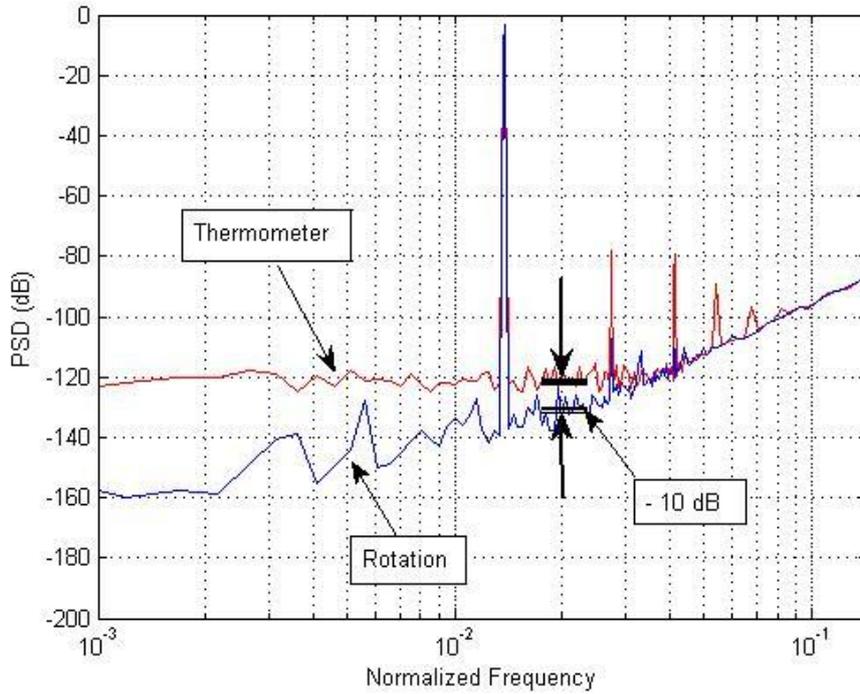
**Fig. (4) : DWA Circuit.**



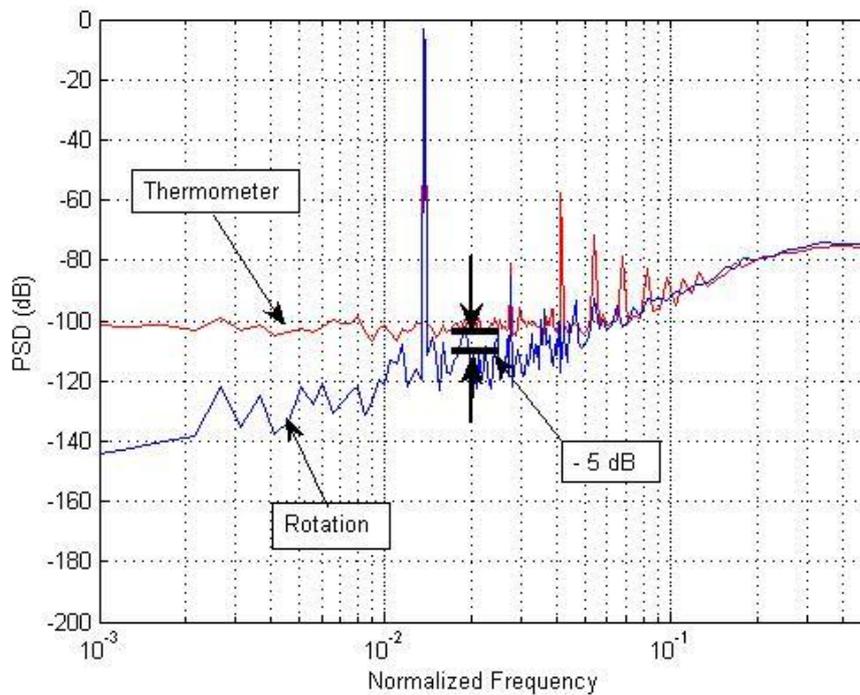
**Fig. (5) : DWA operation.**



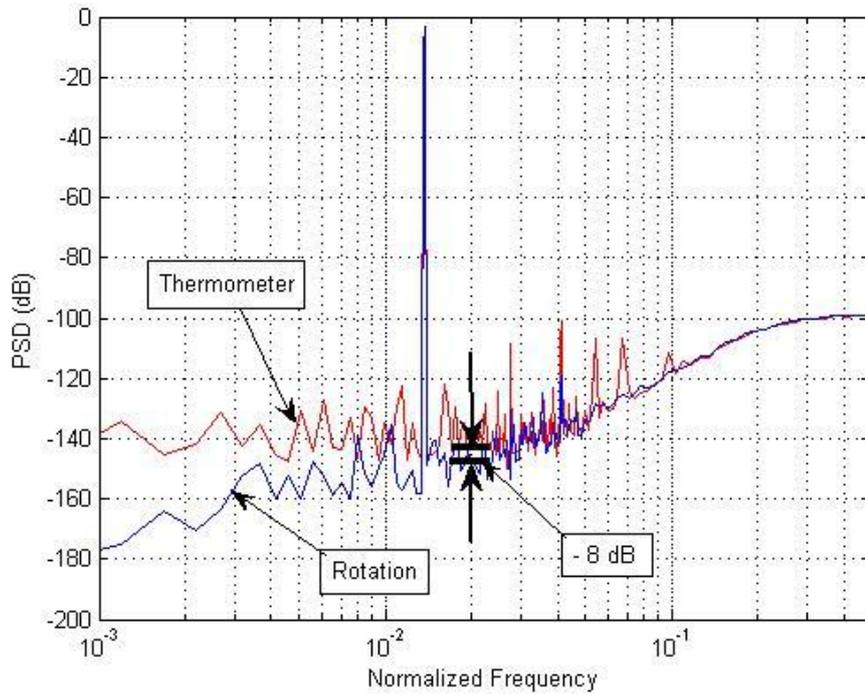
*Fig. (6): The flow chart of the DWA algorithm.*



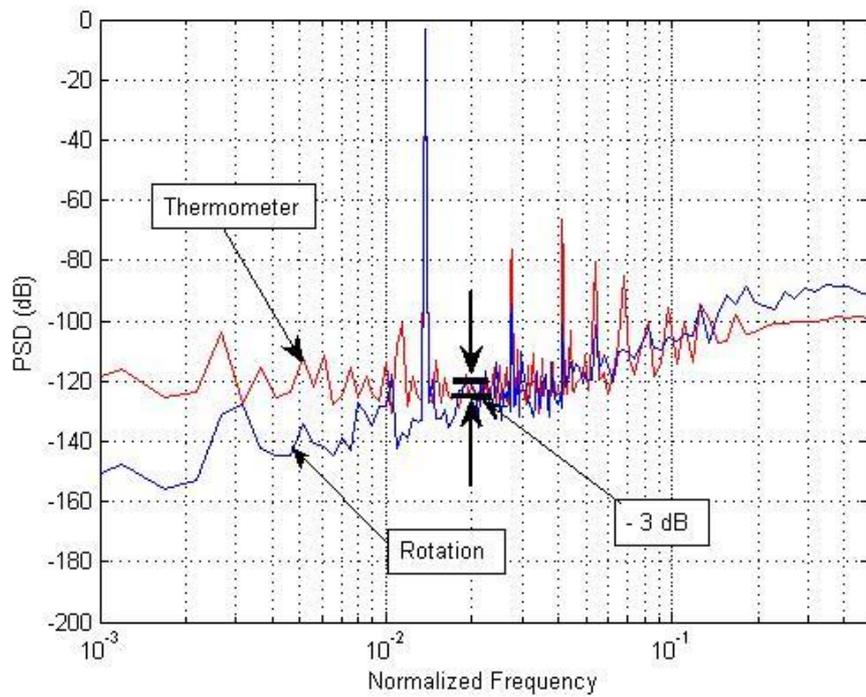
**Fig. (7): Simulation showing the impact of unit element mismatch ( $\sigma = 0.01$ ) with PFD/DAC-8 bit.**



**Fig. (8): Simulation showing the impact of unit element mismatch ( $\sigma = 0.08$ ) with PFD/DAC-8 bit.**



*a*



*b*

**Fig. (9): Simulation showing the impact DWA on the quantization noise spectrum for PFD/DAC-12 bit (a)  $\sigma = 0.01$  (b)  $\sigma = 0.08$ .**

## References

- [1].S. Fili, "Fixed, Nomadic, Portable and Mobile Applications for 802.16-2004 and 802.16e WiMAX Network", WiMAX Forum, November 2005, [www.wimaxforum.org](http://www.wimaxforum.org).
- [2].Y. Tian and I. Chu, "Seamless Mobile Lifestyle Through WiMAX", Motorola, Inc., and De Paul University, 2007. [www.4shared.com](http://www.4shared.com).
- [3].Dixon, "Spread Spectrum Systems", John Wiley & Sons, Inc., 1976.
- [4].K. Shu and E. S. Sinencio, "CMOS PLL Synthesizers: Analysis and Design", Springer, Inc., 2005.
- [5].B. G. Goldberg, "Digital Frequency Synthesis Demystified: DDS and Fractional-N PLLs", LLH Technology Publishing, 1999.
- [6].S. E. Meninger and M. H. Perrott, "A Fractional-N Frequency Synthesizer Architecture Utilizing a Mismatch Compensated PFD/DAC Structure for Reduced Quantization-Induced Phase Noise", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 50, No. 11, page: 839-849, November 2003.
- [7].S. E. Meninger, "Design of a Wideband Fractional-N Frequency Synthesizer Using CppSim", May 2005, <http://www.mit.edu/researchgroups/perrottgrouptools.html>.
- [8].K.Chen and T. Kuo," An Improved Technique for Reducing Baseband Tones in Sigma-Delta Modulators Employing Data Weighted Averaging Algorithm Without Adding Dither", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 46, No. 1, January 1999, pp 63-68.
- [9].E. Bach, "Multibit oversampling D/A converters using dynamic element matching methods", Siemens Corp., Technical Report: Sysconv 27.727, 1999.
- [10].Z. Zhang and G. C. Temes, "A Segmented Data-Weighted-Averaging Technique", IEEE press, Center for Design of Analog-Digital Integrated Circuits (CDADIC), 2007, pp 481-484.

ينضمن هذه البحث مقترح لأستخدام خوارزمية (DWA) من الدرجة الأولى مع مضمن (Sigma-delta) من الدرجة الثالثة لتحسين أداء مركب التردد من نوع (Sigma-Delta Fractional-N) لمنظومة WiMAX. إضافة إلى ذلك تم مناقشة مشكلة عدم التوليف بين عناصر محول الإشارة الرقمية إلى الكمية (DAC). نتائج المحاكاة بينت فعالية تقنية DWA في تقليل مستوى التردد الطيفي وكذلك التغلب على مشكلة عدم التوليف بين عناصر (DAC). مستوى الضوضاء الكسرية تم تحويله إلى الحزمة العريضة. تم تحسين الضوضاء الكمية بمقدار (10 dB-) عندما تكون قيمة عدم التوليف (0.01) و مقدار (-5dB) عندما يكون قيمة عدم التوليف (0.08). تم استخدام برنامج Matlab (V.7) في محاكاة.