Effect on Rapid Thermal Oxidation process on Electrical Properties of Porous Silicon

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Received on:24/6/2008

Accepted on: 9/10/2008

Abstract

In this work, the porous silicon was prepared by using stain etching in HF-HNO_3 at different etching times. Then Rapid Thermal Oxidation (RTO) processes were used for surface treatment at different temperature and oxidation time to enhancement sample properties. Fourier Transforms infrared (FTIR) spectrum exhibit the formation of SiH_x (x=1, 2) and Si-O bonds which indicate the present of porous structure and formation of oxidation porous layer. The Capacitance – Voltage characteristics reveal that effective carrier density is $36*10^{15}$ cm^{-3} for sample etching time at 2min, while there was a change from ($37.8*10^{15}$ to $45.7*10^{15}$) cm^{-3} for sample oxidation at different oxidation temperature (373 – 973)K and from ($38.2*10^{15}$ to $40*10^{15}$) cm^{-3} for sample oxidation at different oxidation time (0.5 – 3.5)min. Also the porosity was (45.56%) for PS/p-Si etching at 2min while reduce from (45% to 35.4%) with oxidation temperature, and from (44.2% to 40.5%) with oxidation time. From photocurrent characterized, that the photosensitivity for PS/p-Si structure is better where etching time at 2min, and its 0.2545 A/W at 370nm, and it increased after Rapid Thermal Oxidation (RTO) from (0.34 to 0.44) A/W with different oxidation temperature, and changed from (0.35 to 0.34) A/W with different oxidation time, so that sandwich hetrojunction exhibit good efficiency photodiode.

Key words: Porous silicon, RTO porous silicon, Heat treatment porous silicon

تاثير عملية الاكسدة الحرارية السريعة على الخصائص الكهربائية للسيليكون المسامي

الخلاصة

في هذا البحث تم تحضير السليكون المسامي بواسطة الطريقة الكيميائية في خليط من حامض الهيدروفلوريك وحامض النتريك عند أزمان قشط مختلفة. ثم معالجة السطح بواسطة عملية الأكسدة الحرارية السريعة عند درجات حرارة وأزمان أكسدة مختلفة لتحسين خصائص النموذج. أطياف FTIR تبدي الأواصر SiH_x (x=1,2) و Si-O التي تشير إلى تكون الطبقة المسامية للسليكون وتكون طبقة الاوكسيد على السليكون المسامي. خصائص سعة-فولتية تعطي كثافة الحاملات $36*10^{15}$ cm^{-3} للعينة عند زمن قشط 2 min, بينما تتغير من ($37.8*10^{15}$ cm^{-3} الى $45.7*10^{15}$ cm^{-3}) لنماذج موكسدة عند درجات حرارة مختلفة K (373 – 973) , وتتغير من ($38.2*10^{15}$ cm^{-3} الى $40*10^{15}$ cm^{-3}) لنماذج موكسدة عند أزمان أكسدة مختلفةmin(0.5 – 3.5). أيضا المسامية تكون (45.56 %) للسليكون المسامي عند زمن قشط 2 min بينما تقل من(45 %) الى (35.4 %) مع تغير درجات حرارة الأكسدة,وتتغير من(44.2 %) الى (40.5 %) مع تغير أزمان الأكسدة. من خصائص التيار الضوئي, أفضل استجابية للسليكون المسامي عند زمن قشط 2 min كانت 0.2545 A/W عند 370 nm , وزادت بعد الاكسدة الحرارية السريعةمن (0.34A/W الى0.44 A/W) مع درجات أكسدة مختلفة , وتغيرت من (0.35A/W إلى 0.34A/W) مع أزمان أكسدة مختلفة, لذا فالتركيب يبدي كفاءة جيدة للدايودات الضوئية.

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1. Introduction:

The resent discovery of room temperature visible luminescence from porous silicon has raised a great deal of interest and effort on porous silicon and related materials. Traditionally, crystalline silicon (c-Si), the heart of modern computer and electronic industry, is an indirect semiconductor with a band gap near 1.1eV at room temperature, and can emit weak light via phone assistance only in the near infrared region. This fact limits silicon applications in optoelectronics, where compound semiconductor with direct band gaps, such as GaAs, InP, and so on, are the dominant materials at present. The difficulties in combining these compounds with the well-developed Si, integrated technology hinder further application and developments. However, the observations of bright visible photo-luminescence and electroluminescence from porous silicon and related materials have changed this trend. Since 1990 papers and reports have opened the door for silicon to play a role in optoelectronic. [1]

Porous silicon is a very promising material due to its excellent mechanical and thermal properties, its obvious compatibility with silicon based microelectronic and its low cost. Also its large surface area within a small volume, its controllable pore sizes, its convenient surface chemistry, and the ability to modulate its refractive index as a function of depth makes porous silicon suitable dielectric material for the formation of multilayer. All these features lead, on one hand, to an interest in optical properties by mixing silicon with air in the effective medium approximation. On the other hand the pores allow the penetration of chemical and biological substances, liquids cells molecules to change *i.e.* the optical behavior of the original system. These effects inspired research into different applications like optical sensing application and biomedical application.

One of the most popular techniques that are used to produce porous silicon is the stain etching process (chemical etching) of silicon wafer in hydrofluoric acid (HF) and HNO3, without applying external potential. The porous silicon prepared in this technique exhibits optical and electrical properties, with different optoelectronic device including photodetectors, solar cells and display devices. [2]

Heating of porous silicon to high temperature in a strongly oxidatizing ambient (for example pure oxygen) leads to vary rapid oxidation of the structure. [3] Rapid Thermal Oxidation of porous silicon makes it suitable as dielectric layer for any electronic device. Most of its applications involve the formation of stable SiO2 layers obtain by a simple technological process like thermal oxidation [4]. Oxidation of porous Si at high temperature is conveniently carried out by the use of rapid thermal oxidation (RTO); involving transient heat of oxygen ambient so that careful control of the potential rapid surface reaction can be maintained.

Rapid thermal Oxidation process divides into two types: [5] Dry Oxidation Thermal which obtain by existing dry oxygen O_2, and Wet oxidation Thermal which obtain by existing vapor water H_2O . Thermal oxidation growth by dry oxygen has the best electrical properties and nearly empty from the dopes compared with the oxides growth by wet oxygen,[5-9] but the limit time to grow to the same thickness at limit temperature longer than for the dry oxygen

Thermal oxidation growth by Rapid Thermal Oxidation (RTO) technique has the best electrical properties like stability films, less current leakage and high breakdown voltage compared with conventional oxidation [10].

In this work, porous silicon was prepared by using stain etching and then RTO process used for surface treatment at

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different temperature and oxidation time to enhancement electrical properties of prepared sample.

2. Experimental sit-up:

Porous silicon was prepared by using silicon wafer p – type (111), which rinsed by using acetone and ethanol in order to remove dirt and oil, while native oxide layer removed by etching in dilute (1:10) HF: H_2O.

Chemical etching which prepared porous silicon using an electrolyte containing 40% HF and HNO_3 (1: 3) acids for different etching time (2, 4, 6, 8, 12) min, Then the samples after that rinsed in ethanol and dried with a jet of nitrogen gas and stored in a container filled with a methanol to avoid the formation of oxides layer on the porous layer.

Rapid Thermal Oxidation of porous silicon samples at different temperatures (373, 473, 573, 673, 773, 873, 923, 973)K with constant time 2.5min, then we chose the beast sample depend on the properties of detector, and oxidation at temperature 923K with different oxidation time (0.5, 1, 1.5, 2, 2.5, 3, 3.5)min. Figure (1) shows a schematic diagram for Rapid Thermal Oxidation system, which consists two parts, the first is Halogen lamp with power (650 watt), and the second part is Quartz tube with diameter (2cm) which is opened from two sides to permit air inter; thermocouple type (k) (NiCr/NiAl), is used to measure the temperature. Halogen lamp connected to varic power supply to control its irradiation intensity according to the required time.

The (Shimadzu-8000) scans of the FTIR measurements are performed over range between (400-4000) cm^{-1} for prepared sample. Surface chemical composition of samples is best probed with Fourier Transform Infrared (FTIR) spectroscopy.

C-V characteristics of the produced hetrojunction were measured using a PM6306 programmable LRC meter supplied by Fluke. The reverse bias voltage was ranged through (0.5 - 5) V. The cross point ($1/C^2$ =0) of the curve represents the built-in potential of the hetrojunction Also there were other parameters could be determine from capacitance measurements such as effective carrier density by using equation (1.1), and depletion layer by using equation (1.2) as following: [11, 12]

$$N_e = \frac{2}{q e_{si} z^2} \frac{dV}{dC^{-2}} \quad (1.1)$$

$$W = \sqrt{\frac{2eV_{bi}}{qN_e}} \quad (1.2)$$

A Kiethley – 616 electrometer was used to measure the flow current in a device manufactured form the produced structure were illuminated by varying high power from halogen lamp and the current was measured in reverse bias with a voltage range of (0.5-8)V, applied from a **Farnell** power supply. This measurement was done for all samples, which prepared at different etching time, and after Rapid Thermal Oxidation processes. The measurement of spectral responsivity were performed using a monochrometer with in range (100-800)nm of wavelength.

3. Result and Dissuasion:

Figure (2) shows the FTIR spectra of PS/p-Si sandwich structure which prepared at different conditions. For all the samples the peaks around (3400 cm^{-1}) are the SiO-H stretching vibration [11], and the peaks around ~3450 m^{-1} are O-H stretching mode [12]. While peaks at (2500-2800) cm^{-1} and peaks at 2300 cm^{-1} [15] are related to Si-Hx (x=1, 2) vibration mode. The peak at ~465 cm^{-1} is related to SiO-Si mode. [16] One can notice that intensity of these bond increases, as temperature and time of oxidation process. This result was agreed with *Leonid et. al.* [17] studies

The capacitance – voltage characteristics of PS/c-Si structure depend on the morphology and the porosity of the etched silicon surface. Figure (3) shows the C-V characteristics of the sandwich structure with different etching time (2, 4, 6, 8, and 12) min. While figures (4) & (5) show the C-V characteristics of the PS/p-Si sandwich structure after RTO for different oxidation temperature and different oxidation time respectively.

The built – in potential V_{bi} can be distinguished from the plot of $1/C^2$ versus V as shown in figures, which obtained from the intersection of the $f(v) = 1/C^2$ plot with the abscissa. Form the slope of the curves, we find the effective carrier density and width of the depletion layer by using equations (2.25) and (2.26) respectively. The results are given in table (1). The value of factor ζ assuming to be 0.2 for p-type silicon substrate [20]. From the result in table (1) (A) the effective carrier density in porous layer change $36*10^{15}\ cm^{-3}$ to $0.3*10^{15}\ cm^{-3}$ for PS/p-Si sample. As etching time increases the pore size increased, and so is the depletion layer width, hence the pore separation increases slowly with the increasing of the pore size, where an increasing pore size results in a lower density film. [18] While changes from $37.8*10^{15}\ cm^{-3}$ to $45.7*10^{15}\ cm^{-3}$ for sample oxidation with different temperature in table (1) (B), and change from $38.2*10^{15}\ cm^{-3}$ to $40*10^{15}\ cm^{-3}$ for sample oxidation with different oxidation time, [see table (1)(C)]. Figure (6) show the variation of porosity (P %) with different etching time. One can notice that the porosity increasing with the increasing of etching time. While figure (7) and (8) explain the variation of porosity (P%) for heterojunction sample after RTO for different oxidation temperature & oxidation time respectively, one can notice that the porosity of sample decreases after RTO process, where it is change from (45%) to (35.4%), with different oxidation temperature and it is change from (44.2%) to (40.5%) with different oxidation time. This behavior is due to the transformation of silicon crystallite into silica which is accompanied by a volume expansion.[19]

Photocurrent represented an important parameter which effected on spectral responsivity, and the linearity of detector properties also quantum efficiency. Figure (9) explains the I-V characteristics sandwich structure under illumination with constant power density $(420)\ mW/cm^2$ at different etching time (2, 4, 6, 8, and 12)min. While figure (10) and (11) shows I-V characteristics after RTO, when the structure was illuminated, the electron – hole pairs generated in the deplation layer of PS/c-Si heterojunction would reduce the barrier for the electrons. These figures show that photocurrent is a function of etching time, and also show that photocurrent increases with different oxidation temperature and with different oxidation time.

After oxidation the doping becomes more electrical activity but at high temperature and high time, defect was generated and work as capture centers for carriers generation, where this less from photo current.

Figure (12) shows the variation of responsivity as a function of wavelength for PS/p-Si prepared at different etching time. Figure (13) and (14) show the spectral responsivity after RTO at different fabrication conditions.

The values of sensitivity change as (0.25, 0.18, 0.135, 0.1, 0.04) A/W by increasing etching time (2, 4, 6, 8, 12)min respectively. This shift is due to the changing in the band gap of the silicon nanocrystallites layer. While figure (13) & (14) show increases the sensitivity after RTO with different oxidation temperature and different oxidation time, The values of peaks of spectral responsivity are (0.34, 0.35, 0.38, 0.47, 0.485, 0.654, 0.49, and 0.44) A/W and the peaks are at different oxidation temperature. While its peaks are (0.35, 0.4, 0.41, 0.582, 0.48, 0.47 and 0.43) A/W at different oxidation time. This due to the reduction of the resistivity of these structures, which cause an

increasing of the electrical conductivity and then increasing in the photocurrent as a function of responsivity.

4. Conclusions

The main conclusions can be summarized as follows:

1. The present work was successful to prepare porous silicon by stain etching at different etching time. It is simple and controllable process with low cost.
2. FTIR spectrum exhibit the formation of SiHx (x=1,2) and Si-O bonds, which was increased after RTO process.
3. The capacitance – voltage depends on the porosity, which is a function of etching time. After Rapid Thermal Oxidation, we showed that the porosity was reduced.
3. The current – voltage characteristics of sandwich structure enhancement after RTO, for different oxidation time, and different oxidation temperature.
4. The results of spectral responsivity increasing after RTO for different temperature and oxidation time.

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Table (1) (A): Experimental result of porous silicon hetrojunction at different etching time

PS/P-Si Etching time(min)	V_{bi} V	N_e cm^{-3}	W μm
2	0.4	$36*10^{15}$	1.7
4	0.3	$24.9*10^{15}$	3.2
6	0.2	$7.6*10^{15}$	4.3
8	0.5	$2.9*10^{15}$	4.9
12	0.1	$0.3*10^{15}$	4.5

(B): Experimental result of PS/p-Si hetrojunction after RTO for different oxidation

RTO (PS/p-Si) Temperature(K)	Ne cm^{-3}	V_{bi} V	W Mm
373	$37.8*10^{15}$	0.2	1.6
473	$39.7*10^{15}$	0.15	1.4
573	$43*10^{15}$	0.23	1.1
673	$59*10^{15}$	0.13	0.7
773	$62*10^{15}$	0.1	0.4
873	$75*10^{15}$	0.25	0.26
923	$55*10^{15}$	0.6	0.6
973	$45.7*10^{15}$	0.4	0.75

(C): Experimental result of PS/p-Si hetrojunction for different oxidation time at 650Ċ.

RTO (PS/p-Si) Time(min)	Ne cm^{-3}	V_{bi} V	W Mm
0.5	$38.2*10^{15}$	0.4	1.64
1	$44*10^{15}$	0.2	1.47
1.5	$53*10^{15}$	0.15	1.18
2	$65*10^{15}$	0. 3	0.58
2.5	$55*10^{15}$	0.6	0.6
3	$49*10^{15}$	0.4	0.8
3.5	$40*10^{15}$	0.2	0.92

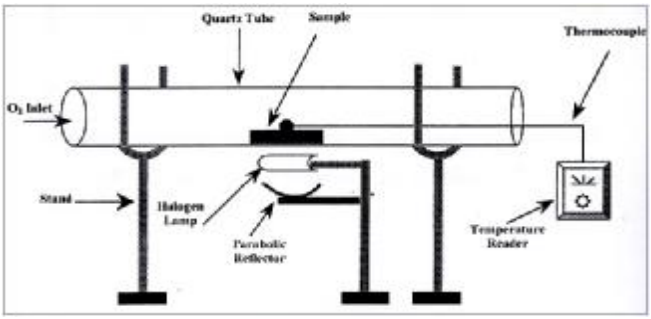

Figure (1) Schematic diagram of Rapid Thermal Oxidation RTO system

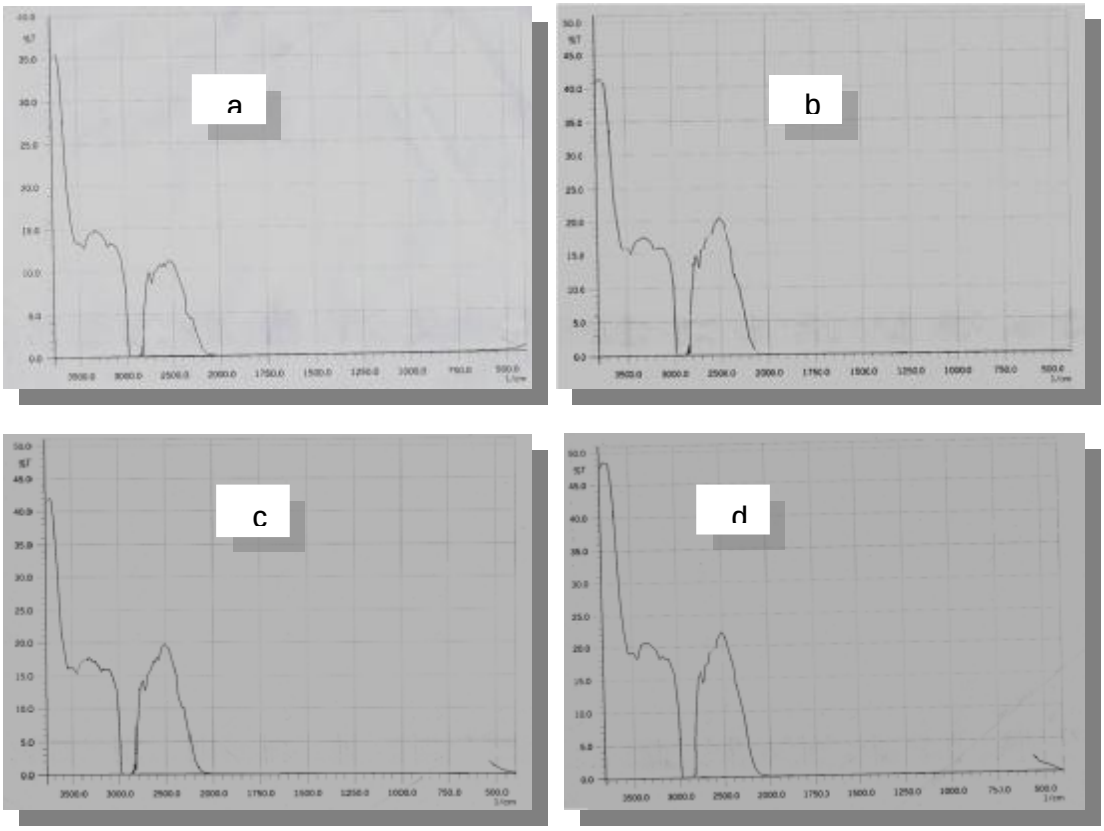

Figure (2): FTIR spectrum: a. for porous silicon before RTO. b. porous silicon after RTO at 573K and 2.5min. c. porous silicon after RTO at 773K and 2.5min. d. porous silicon after RTO at 773K and 3.5min.

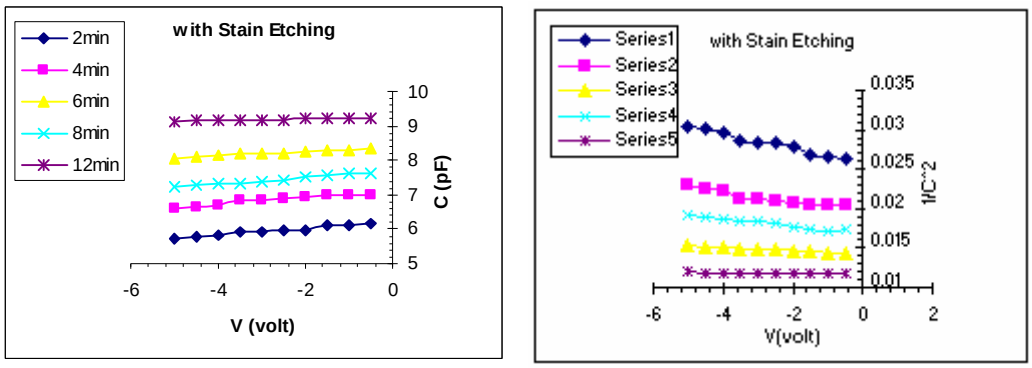

Figure (3) C-V characteristics of the structures with etching time (2, 4, 6, 8, and 12) min.

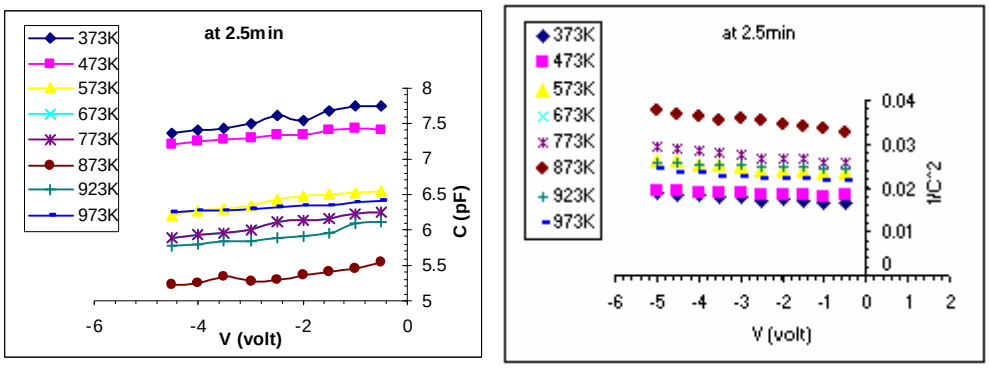

Figure (4) C-V characteristics of the structures after RTO at constant time 2.5min with different oxidation temperature.

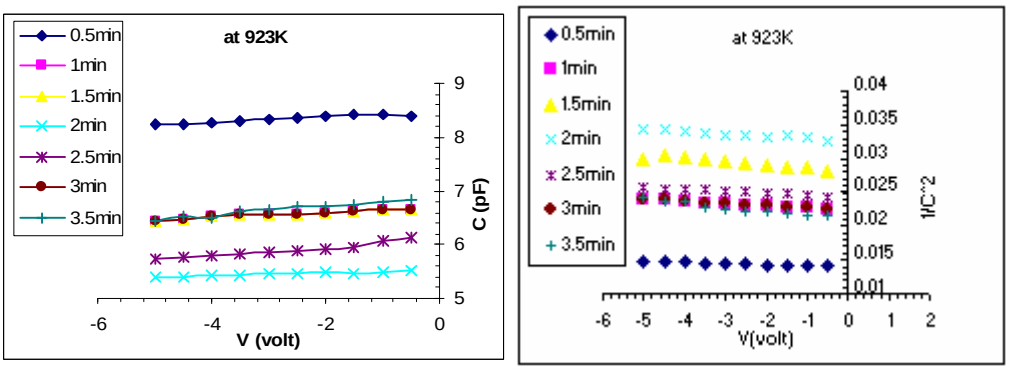

Figure (5) C-V characteristics of the structures after RTO at constant temperature 923K with different oxidation time

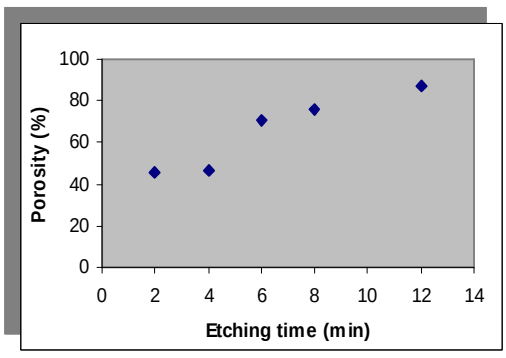

Figure (6) The relationship between etching time and porosity.

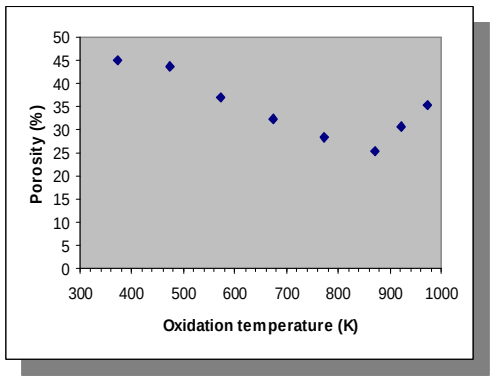

Figure (7) The relationship between oxidation temperature and porosity.

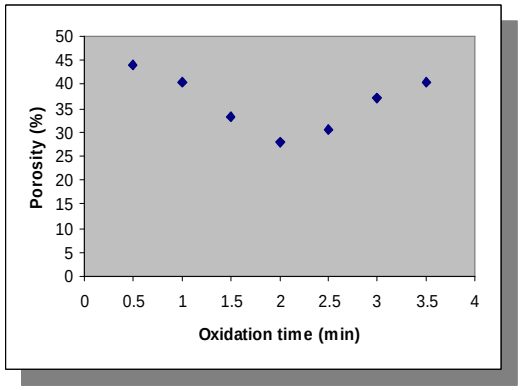

Figure (8) The relationship between oxidation time and porosity

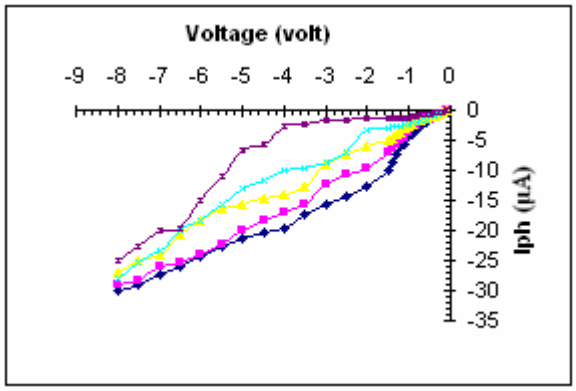

Figure (9) Photocurrent of PS/p-Si heterojunction as a function of reverse bias illuminated power density (420)mW/cm2 for different etching time 2min (—◆—),4min (—■—),6min (—▲—), 8min (—+—), 12min(—✳—).

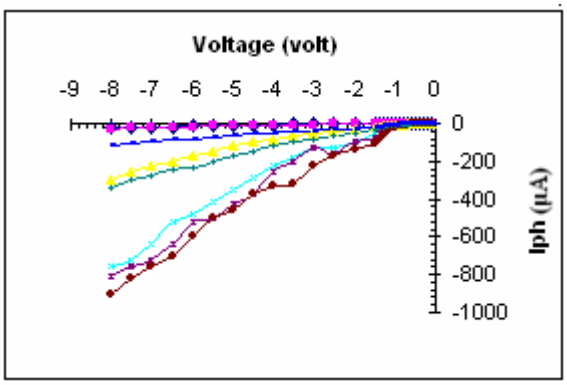

Figure (10) Photocurrent of PS/p-Si heterojunction as a function of reverse bias illuminated power density (420)mW/cm2 after RTO at different oxidation temperature 373K( ), 473K( ), 573K( ), 673K ( ), 773K ( ), 873( ), 923K ( ),973K ( ) and constant oxidation times 2.5min.

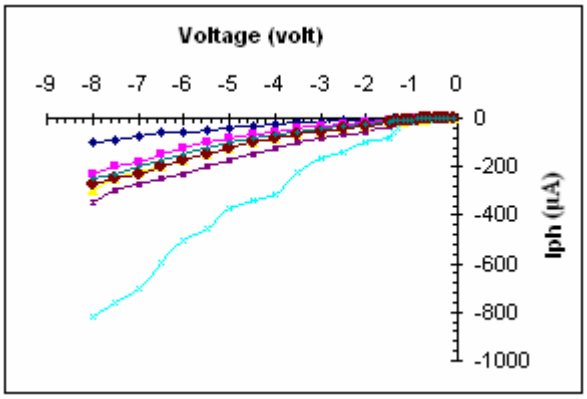

Figure (11) Photocurrent of PS/p-Si heterojunction as a function of reverse bias illuminated power density (420)mW/cm2 after RTO at different oxidation time 0.5( ), 1min( ), 1.5min( ), 2min( ), 2.5min ( ), 3min ( ), 3.5min ( ), and constant oxidation temperature 923K.

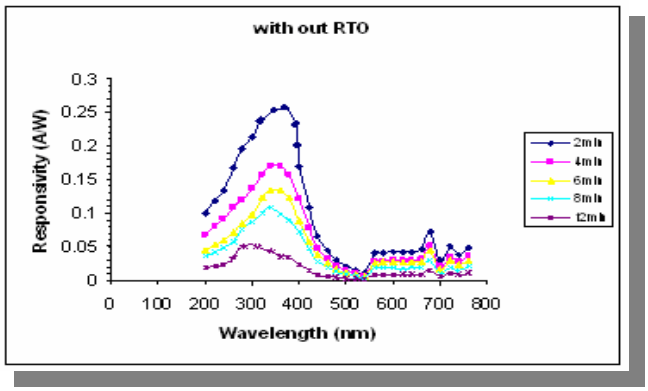

Figure (12) Spectral Responsivity of PS/p-Si samples prepared at different etching time.

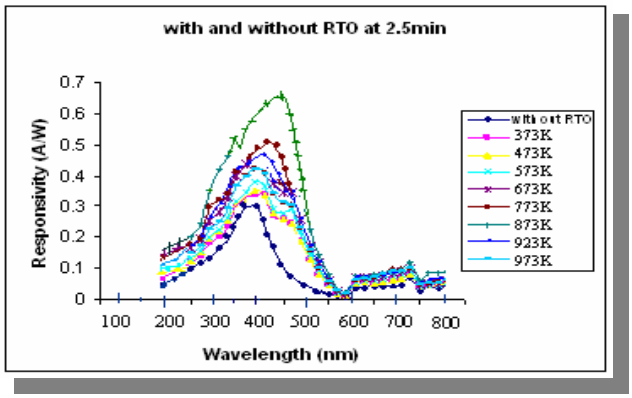

Figure (13) Spectral Responsivity of PS/p-Si samples after Rapid Thermal Oxidation RTO prepared at different oxidation temperature with constant time 2.5min.

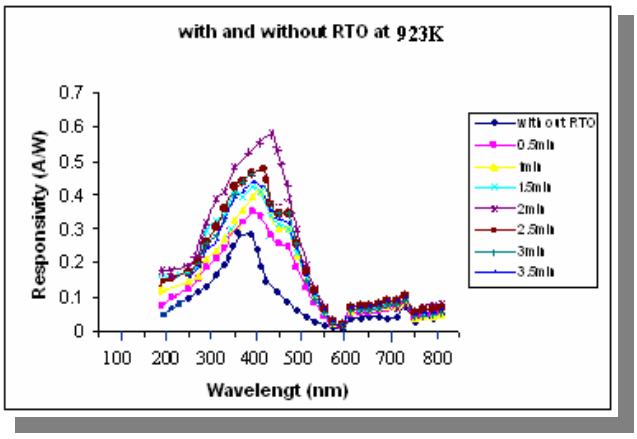

Figure (14) Spectral Responsivity of PS/p-Si samples after Rapid Thermal Oxidation RTO prepared at different oxidation times with constant temperature 923K.