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DESIGN AND SIMULATION OF THREE STAGES DECIMATION FILTER FOR WCDMAUSING FDATOOL IN MATLAB

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Abstract: The design and simulation of the digital decimation part for wideband code division multiple access (WCDMA) based software defined radio (SDR) technology is presented in this paper. A system level design tool, SIMULINK and FDAToolan environment in MATLAB is adopted together in the design sequence to give digital decimation higher efficiency. The proposed decimation filter includes three cascaded FIR filters. The residual sub modules of the decimation filter, such as FIR filters, participated in its design using MATLAB with the trade-offs between the considerations to get through the requirements of WCDMA, and the complexity of the algorithm and simulation. Finally, the decimation filter is simulated on MATLAB SIMULINK block set and its performance is also addressed and tested using FDATool and that supports current and future generation of wireless and mobile systems.

Keywords: *Decimation Filter, WCDMA, SDR, MATLAB.*

تصميم ومحاكات مخمد ترشيح لمنظومة دبل يو سي ديي ام اي باستخدام برنامج ماتلاب

الخلاصة:هذا البحث يعرض تصميم ومحاكات الجزء المخمد الرقمي لمنظومة دبل يو سي دي ام اي بالاعتماد على تكنلوجيا الراديو المعرف برمجيا. تم اعتماد وتبني عدة برامج مثل سميولنك ومختبر تصميم الفلتر الرقمي المتوفر في برنامج ماتلاب لزيادة كفاءة التصميم. يتكون المخمد المقترح من ثلاثة مراحل لمرشحات رقمية مربوطة على التوالي مع بعضها لاخماد الاشارة. مكونات المرشح المخمد مثل المرشحات ذات الاستجابة المحدودة تم تصميمها لتلبية متطلبات النظام مع الاخذ بنظر متطلبات المستلمة وتعقيد المحاكات. اخيرا تم محاكات المرشح المخمد باستخدام برنامج ماتلاب وتم تقييم عمل وتصرفات المرشح باستخدام مختبر تصميم المرشحات الرقمية والذي يدعم الجيل الحالي والمستقبلي للأنظمة اللاسلكية والمتنقل.

1. Introduction

The wireless interface technology of multiple wireless communication standards can be implemented into a single transceiver system is called software defined radio (SDR) [1]. The majority of the functional blocks including RF signal processing blocks are achieved by a software module implemented with a high-speed processing unit in

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SDRconcept. A single hardware platform can hold multiple wireless communication standards without replacing hardware components.

The services change according to customer preferences and real-time acceptance of new services can be made on the fly by downloading new application software. To provide updated wireless standards and protocol software later on through downloading once can sell SDR transceivers. One can quickly become accustomed to the evolving communication marketplace and maintain their competitiveness. Therefore, SDR, which enables multimode, multiband, and multi-function through a software upgrade, is expected to be one of the most important mobile [2].

Decimation process is one of the vital signs processing tasks to receive WCDMA and plays a big task in achieving the communications systems of 3G and 4G. It's used to decrease the frequencies from Intermediate frequency (IF) baseband. It also leads to the bottom of the converter and filter matched. It is known widely that the FPGA is one of the best options for the implementation of this filter [3]. Although the implementation in FPGA decimation filter is not an easy task for the designers Euenbga to be aware of too many factors, such as HDL coding algorithm, energy consumption and so on. Fortunately, designers can use the XILINX System Generator tool to achieve the goal of a more efficient design [4].

2.System Requirements

The Decimation part must be designed to satisfy the WCDMA specification [2], which sets out the terms and receive radio base station transfer. Table 1 shows a summary of the necessary path to meet the needs of broadcast receiver.

Table 1. Specifications for receiving transmissions Path [2]

Parameter	Value
Carrier B.W	5.0 MHz
Number of carrier	1
DUC sample rate	61.44 MCPS
DDC Output rate	7.68 MSPS
Input Signal Quantization	14-bit
Output Signal Quantization	16-bit I and Q

3.Decimation Filter Design

The modules of decimation filter have to design in complete WCDMA requirements [5], which is obtained from the specifications Generation Partnership Project 3 [6]. Entrance to the decimation filter samples is a real signal of 61.44 MSPS and quantity to 14 bits. Output and production complex baseband and be at a sampling rate of 2 * F = 7.68 MSPS chip where the chip frequency is 3.84 MSPS. As a result, there is a need to 61.44 / 7.68 = 8 factor, which can be achieved in a few ways. Usually occur, it is best to perform decimation in a series of stages rate is smaller than it was at one stage with a

large rate of change [7]. There are reasons from the point of view of both system design and hardware implementation. In the design of the system, change the results and the smallest rate in the transformation of the band on a larger scale, which leads to the taps, much less in the filter design From the perspective of hardware implementation, and use multiple stages makes a later stage, the destruction of working in less sample rate. Therefore, the use of devices to destroy complex less than one stage, and computational efficiency is increased dramatically. Moreover, the successive stages of the liquidation of a broader gangs moving in a row.

Decimation and interpolation by a factor of require low pass filters with cutoff frequency Wc = π / 2 , that is , ideal half-band filters .

The impulse response of this h[n] = $\frac{Wc}{\pi}\frac{SinWc(n-\propto)}{Wc(n-\propto)}$ $|_{W_C = \pi/2} = \begin{cases} 1/2 , & n=\alpha \\ 0 , & n-\alpha = \pm 2, \pm 4, \ldots \end{cases}$ To simplify the discussion we assume α = 0 , that is , we consider noncausal zero-phase filters with real frequency response function H(e^{jw}) , In this case ,we have

h[0] = 1/2 , h[2n] = 0 , n = ±1 , ±2 ,…

Thus the poly phase representation of $H(z) = \sum_{K=0}^{M-1} h[k]\ Z^{-k} = \sum_{K=0}^{D-1} Pk(Z)\ Z^{-k}$

Is given by $H(z) = Po(z^2) + z^{-1}P1(z^2) = 1/2 + z^{-1}P1(z^2)$

$Po(z) = \sum_n h[2n]z^{-n}$ $P_1(z) = \sum_n h[2n+1]z^{-n}$

In general , any filter with h[-n] = h[n] or $H(e^{-jw}) = H(e^{jw})$

That satisfies h[0] = 1/2 , h[2n] = 0 , n = ±1 , ±2 ,… is called a half-band[8].

Based on the above considerations, we designed three half-band FIR filters and the bottom of the samples of the two decimation filter to perform the operation. The graph shows a mass of WCDMA decimation filter in Fig. 1.

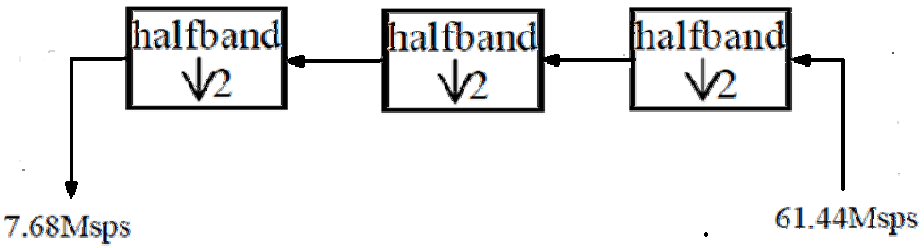

Figure 1. WCDMA decimation Block Diagram

3.1. Half-Band Decimation Filters

Tational burden of work dramatically [10]. In our design, it has been designed decimatiafter the frequency translation, it is used to the loss of three half-band for a series of filters to reduce the sampling of 61.44 medium-sized projects to the average medium-sized enterprises 7.68. Band half-filters are a type of filters FIR which passband ripples stopband are the same, and passband edge and one edge frequencies than half the distance Size-P / 2 frequency stopband option to implement the filter with two structure is usually the rate because every indexing coefficient strange time field zero except the center tap and even indexed transactions symmetric [9].

This feature reduces the compuon band filters using three half Equiripple roads with a factor of two, both on the basis of the consideration of the trade-off. The main criteria for half a detailed three-band filters in Table 2.

Table 2.Specifications Summary of Half-band Filters.

Filter Stage	**First**	**Second**	**Third**
Passband Fpass (MHz)	2.34	2.34	2.34
Sample Rate F (MHz)	61.44	30.72	7.68
Filter Order	10	18	94
Peak – to – Peak Ripple (dB)	0.0001	0.0001	0.0001
Stopband Attenuation (dB)	100	100	100
Coefficient Quantization	16 bits	16 bits	16 bits
Design Method	Equiripple	Equiripple	Equiripple

The first stage HalfbandEquiripple filter shows a stable impulse response and stable group delay within 11-taps filter length and bandwidth as illustrated in Figure 2 and Figure 3 respectively. Linear phase response within the bandwidth of interest and a fixed delay within the range of bandwidth as shown in Figure 4.linear phase refers to the situation where a linear phase filter response (straight line) function of the frequency [11]. This leads to delays, despite the fact that the current candidate. The same for all frequencies. Therefore, the candidate does not cause distortion or misrepresentation delay stage.

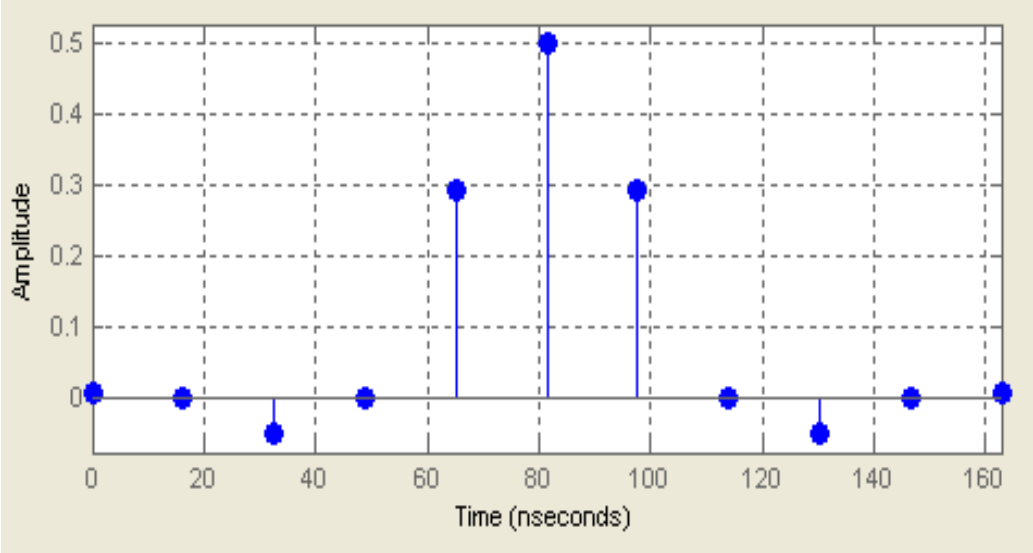

Figure 2: Impulse response of first stage halfband filter

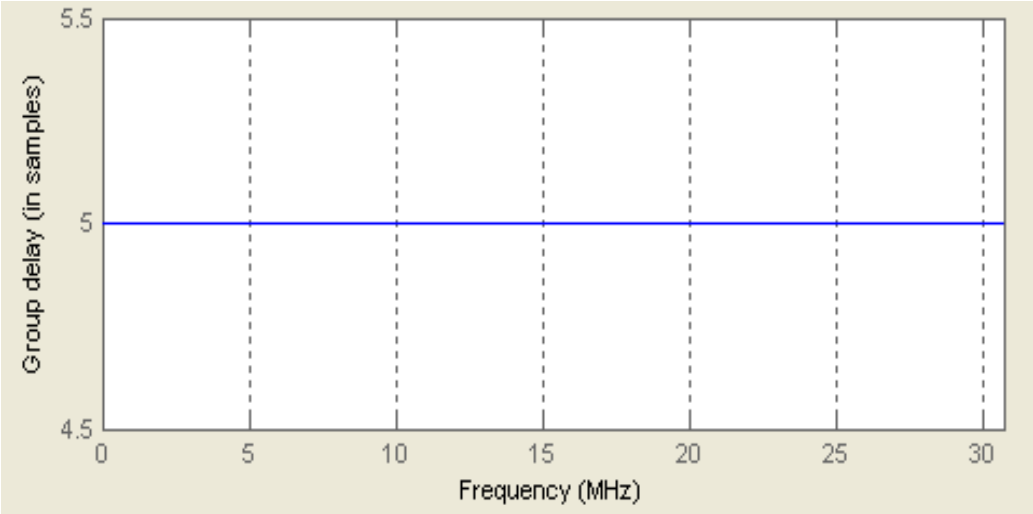

Figure 3: Group delay of First stage halfbandfilte

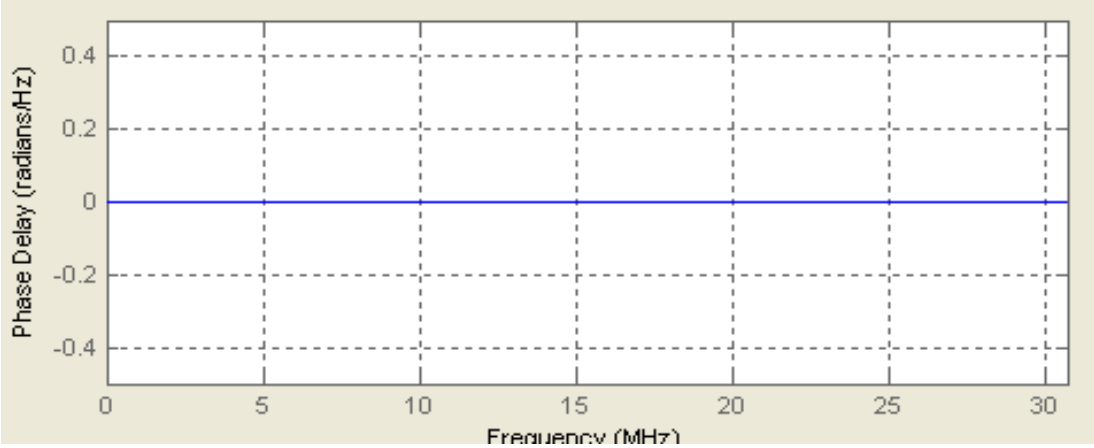

Figure 4: Phase delay of first stage halfband filter

The second and third stage of the proposed decimation filter state that the filters response is stable and the phase and group delay is constant along with bandwidth. The stability of three filters gives a great indication for proposed filter performance and efficiency in the band of interest

The magnitude response of last stage halfbandEquiripple filters shows that the filter provides the WCDMA specification requirements as shown in Figure 5. If one have a look to the filter response in the band of interest 2.34MHz that represent the WCDMA IF specifications, the filter give flat response with no distortion in this band. Therefore, the filter provides the WCDMA requirements as these paper objectives. Finally, the filter provides constant phase and group delay along with band of interest as illustrated in Figure 6 and Figure 7 respectively.

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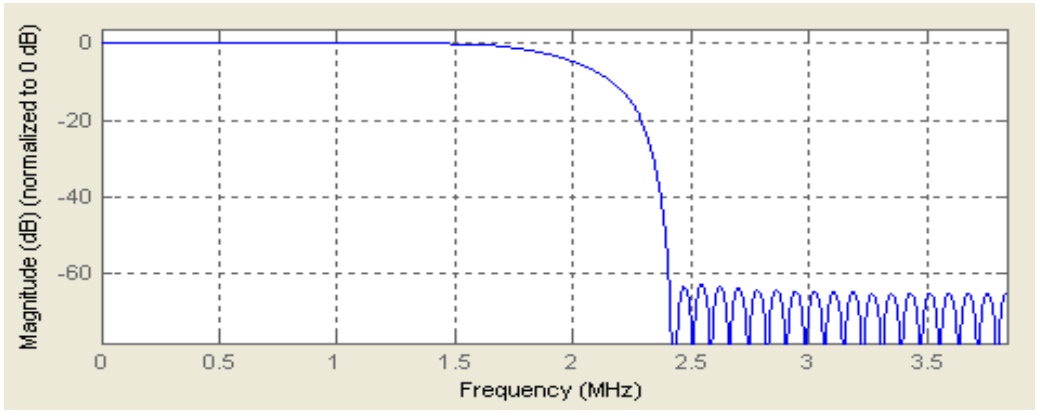

Figure 5: Magnitude response of last stage in filter chain

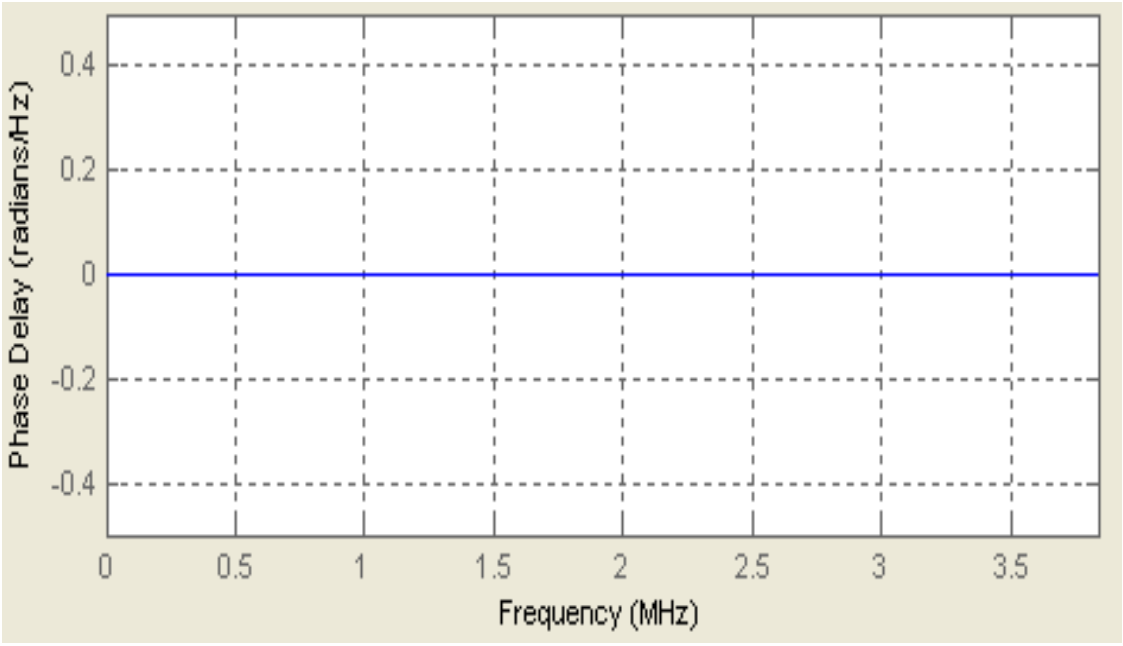

Figure 6: Phase delay of last stage Equiripplefilter

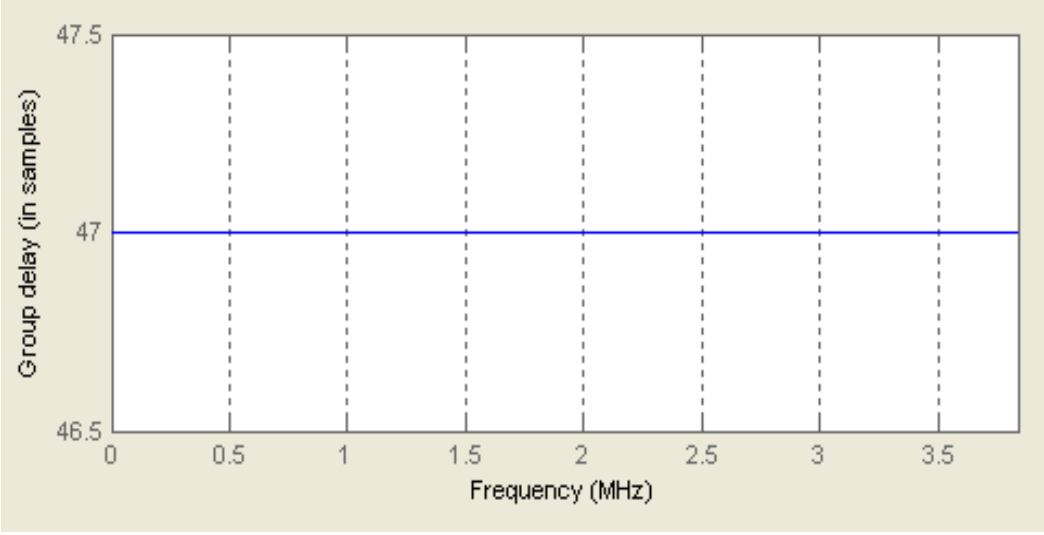

Figure 7: Group delay of last stage Equiripple filter

4. Decimation Modules Simulation

Having designed the three Equiripple decimation filters in MATLAB FDATool [12], [13], [14] then the cascaded of three decimation filter is running in a WCDMA transceiver model as shown in Figure 8.

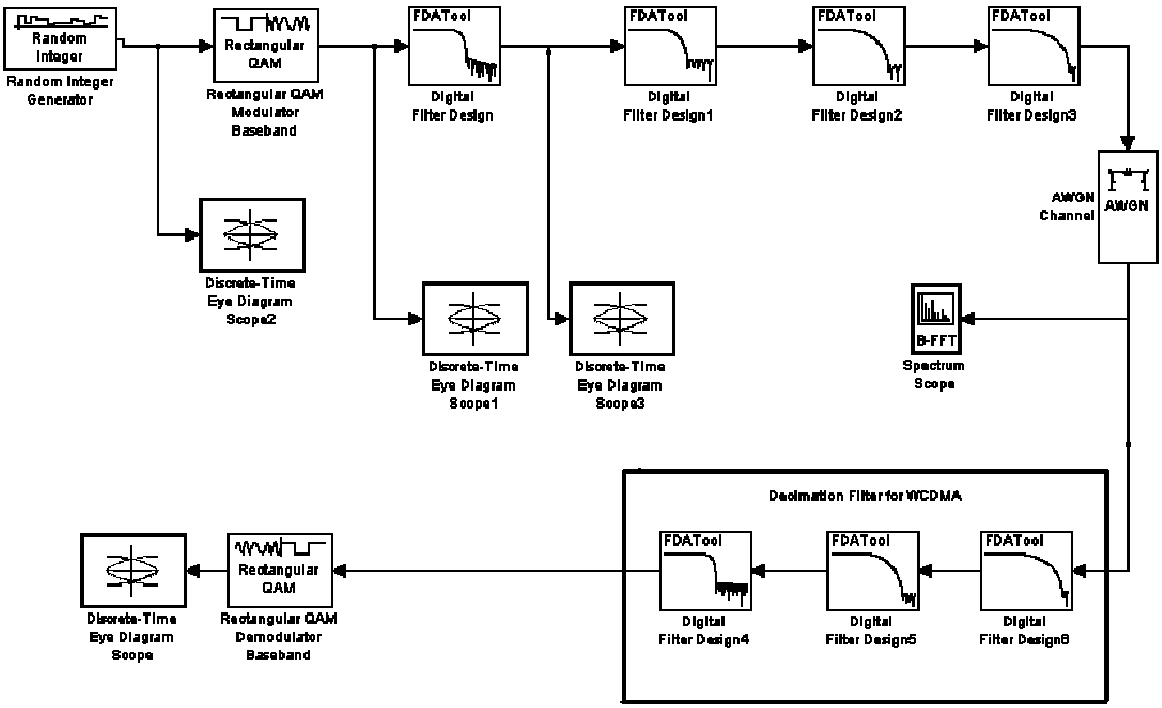

Figure 8: WCDMA transceiver design with three halfband decimation filter modules.

The random integer generator generates the data with sample time of 3.84×10^{-6} frame based output which represent the WCDMA original signals. The rectangular QAM modulates the input signal with in-phase and quadrature channels as shown in Figure 9. And sampling the modulated signal even if the average Duc interpolation spectrum level of the original to be processed under the 20 dB AWGN channels baseband signal as shown in Figure 10. The size of the baseband signal strength of 3 dB.

In the receiver path, the output signal from AWGN channel is pass through the proposed decimation filter to down sample and filtering in same time. The decimation filter consist of three halfbandEquiripple filters is used to down convert the incoming signal from IF band to baseband in order to demodulated and recovered the origin signal. Due to efficient design of the decimation filter, the received signal is free from the channel noise and inters symbol interference (ISI). However, no distortion is found in the output of proposed decimator.

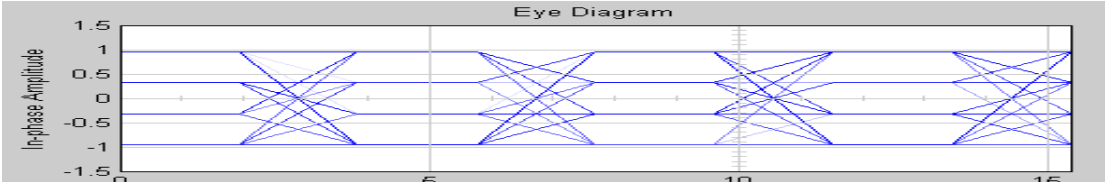

Figure 9.Eye diagram of In-phase and qudrature channels.

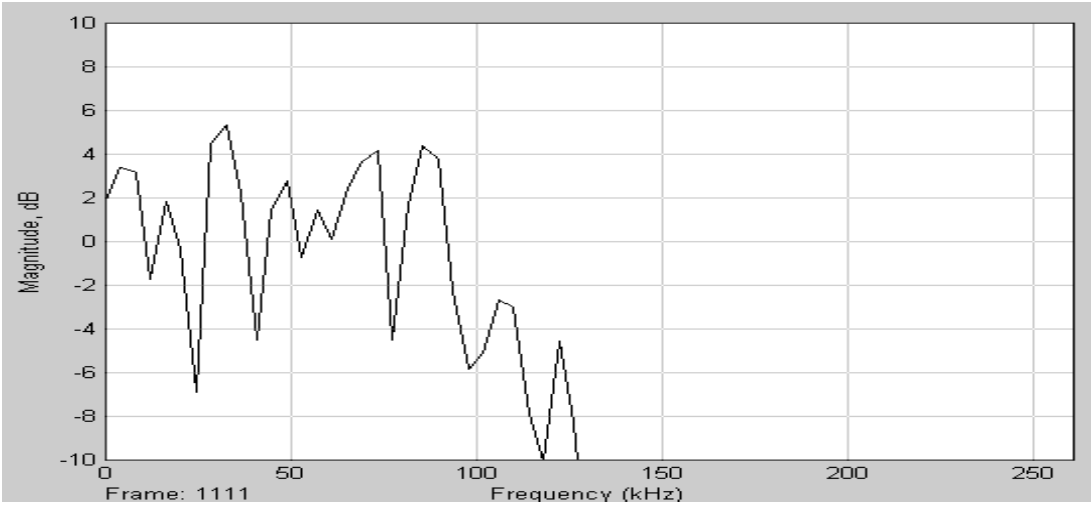

Figure 10: WCDMA Original Baseband Signal.

5.Conclusions

This paper has developed the design of decimation filter system to deal with WCDMA. Design approach is to use MATLAB FDATool to achieve the goal of the design. We discussed the trade-off analysis and system requirements, and the complexity of the algorithm and simulation and analysis. It was found that the proposed design has fulfilled the requirements of WCDMA.

The simulation results shows that all three stages in filter chain is stable and the phase response is constant along with band of interest as well The reform group also delayed also in the bandwidth of the systems as well as WCDMA. Therefore, the proposed algorithms are promising to support the current and future generation of wireless and mobile systems.

6.References

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