FPGA Based Speed Control of a Separately Excited DC Motor

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الملخص

تم التحكم في سرعة محرك تيار مستمر بقدرة 2 كيلوواط عن طريق تغيير الفولتية للجزء الدوار له. تغيير فولتية الدوار انجز عن طريق مغير من نوع (Buck Regulator) . وقد تم التحكم في مفاتيح هذا المغير عن طريق مولد تضمين عرض النبضة (PWM Generator). وقد استخدم (Series Compensator) المتحكم المتوالي في دارة سيطرة مغلقة للتحكم في دورة العمل (Duty Cycle) لمولد تضمين عرض النبضة(PWM). أعتمدت لغة وصف الكيان المادي (VHDL) في تصميم المتحكم المتوالي ومولد تضمين عرض النبضة. أستخدم كارت (XILINX Spartan 3E) المعتمد على دائرة البوابات المبرمجة حقليا (FPGA) ذو الرقم (XC3S500) لتنفيذ المسيطر المطلوب وقد تمت السيطرة بشكل جيد وكفوء.

ABSTRACT

An armature voltage control is used to control the supplied voltage of an armature of a 2 kW separately excited DC motor. A buck regulator is used to vary the supplied voltage of the motor. A pulse width modulation (PWM) generator is implemented to supply the signal to the gate of the switch of the buck regulator. A series or cascade compensator is placed to control the duty cycle of the (PWM) generator in the closed loop control system. Both cascade compensator and (PWM) generator are designed by adopting the very high speed integrated circuit hardware description language (VHDL) and the Xilinx Spartan-3E field programmable gate array (FPGA). The results obtained are in close resemblance with those got from a MATLAB model for the same system.

Keywords: DC motor speed control, PWM, FPGA, Buck regulator, Series compensator.

1. Introduction:

DC motors are widely used due to their performance. The starting torque, for example, in a DC motor can be higher several orders in magnitude than that for a comparable size AC motor; also DC motors can have a wide range of speed control and operate at speeds less or more than the rated speed. There are many applications of DC motors such as (automobiles, boats, computers, airplanes, traction motors, printers, subway trains, etc) [1, 2]. The extensive usage of DC motors in different applications makes speed control of DC motors strongly needed.

DC-DC switching power converters, due to their high-efficiency, are essential parts of the power supply system in many electrical types of equipments [3]. From control point of view, operation of these converters can be considered as a tracking problem, where the output quantity (output voltage, V_o) is required to follow a reference command with low transient and steady state error. To control the armature voltage, a buck converter (step down converter) is used to vary the output voltage from zero to the supply voltage V_s (rated motor voltage).

2. Buck converter:

Choppers have several advantages such as high efficiency, control flexibility, light weight, small size, quick response, and regenerative braking down to low speeds [2, 4]. Buck converter shown in Figure (1) is one kind of the DC to DC converters, which can vary the output voltage from zero to the supply voltage, and its can be explained into two function modes of operation:

Mode one when the switch (S) is closed for a time (t_{on}), the supply voltage will appear across the load resistance (R).

Mode two when the switch (S) is opened for a time (t_{off}), the voltage across the load resistance (R) becomes zero.

The following equation represents the average output voltage of the buck converter (V_o) [2]:

$$Vo = K\,Vs \qquad ...(1)$$

where:
Vo : the output voltage,
Vs : the supply voltage,
K : duty cycle = t_{on}/T , where ($0 \leq K \leq 1$),
and T : the time of one cycle.

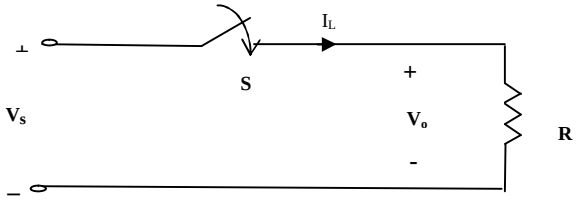
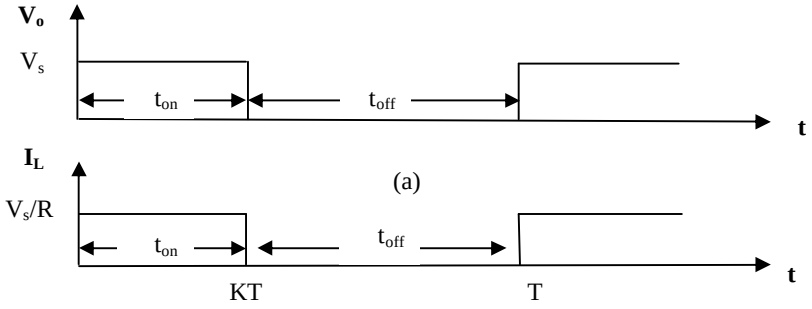


Figure (1): Step down (buck) converter

Figure (2) represents the output voltage and the output current waveforms for a step down converter with a resistive load.



(b)

Figure (2): Step down converter wave forms
(a) The output voltage (b) The output current

If the load is highly inductive (like a DC motor) then the circuit will operate in the continuous mode, and the waveforms are as shown in Figure (3) [2].

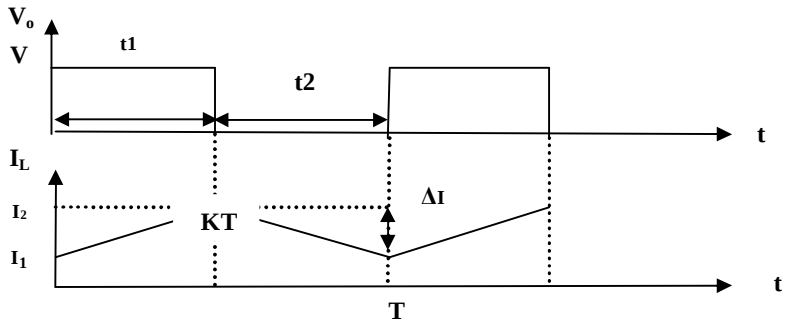


Figure (3): Waveforms of V_o and I_L for step down buck converter supplying a highly inductive load.

In general the buck converter is simple and needs a single transistor and it can produce an output voltage from 0 to V_s . The output voltage of a buck converter can be varied by varying the duty cycle in the PWM signal generator with fixed frequency.

3. Generating the PWM signal:

The PWM signal can be created by comparing a DC reference signal with a sawtooth carrier signal by using a comparator. In this work, a different approach is used to generate the PWM signal which is obtained digitally by using a programmable up-down counter and the counter starts to count from a certain value (digital word) as shown in Figure (4) [5].

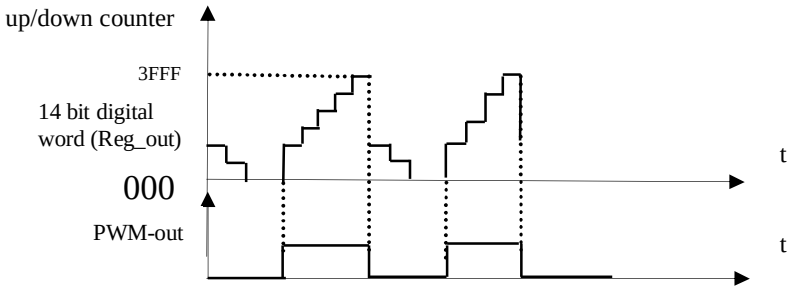


Figure (4): Generating the PWM signal

The PWM output signal is generated periodically with a constant frequency. Sometimes this PWM signal is called Digital PWM (DPWM) [6]. This signal is generated by a VHDL code implemented in (Spartan 3E) FPGA. Figure (5) represents the flowchart of the PWM generator as implemented in (Spartan 3E) FPGA.

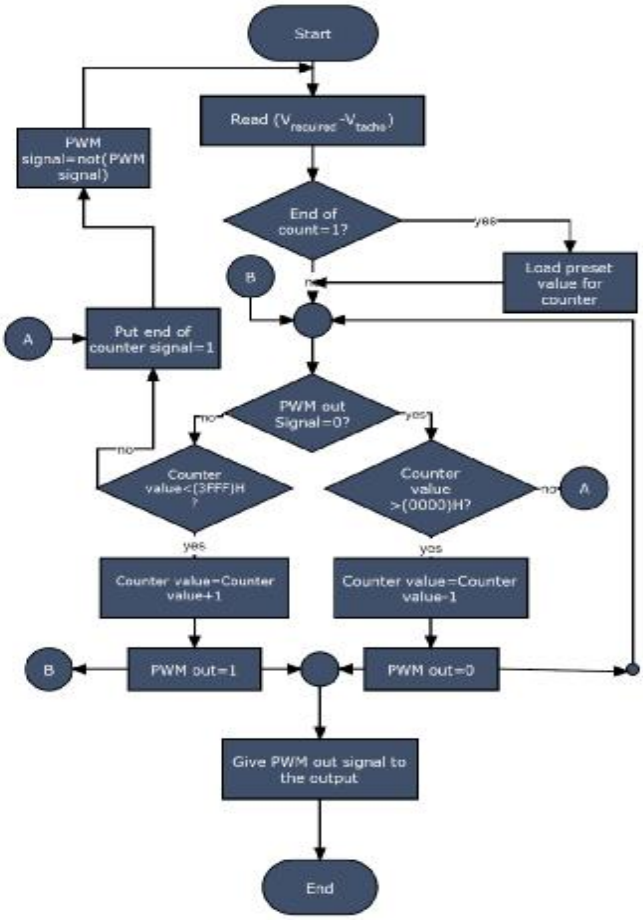


Figure (5): Flowchart for the PWM generator

4. The controller (cascade compensator):

A general block diagram of the designed closed loop system is shown in Figure (6). The controller section consists of a comparator and an up/down counter. The comparator is used to compare between the reference signal (V_{ref} -8bits, coming from external 8-slide switches) and the feedback signal (V_{tac} -8bits, coming from ADC). If (V_{ref}) is greater than (V_{tac}), the counter will count up. If it is less, then the counter will count down, while when (V_{ref}) equals (V_{tac}), the counter will stay on its current value.
The calculations for the output frequency (switching frequency) and the duty cycle depend on the number of counter bits (n). The following equations can be used for switching frequency calculations [5]:

$$t_{sw} = T_{clk} * 2^n \quad \ldots (2)$$

$$f_s = \frac{1}{t_{sw}} \quad \ldots (3)$$

$$K = \frac{\text{set point}}{2^n} \quad \ldots (4)$$

where: t_{sw} : the switching time.
n : the number of counter bits.
T_{clk} : the FPGA clock time period.
f_s : the switching frequency.
K : the duty cycle.

and Set point : digital word placed by external switches.

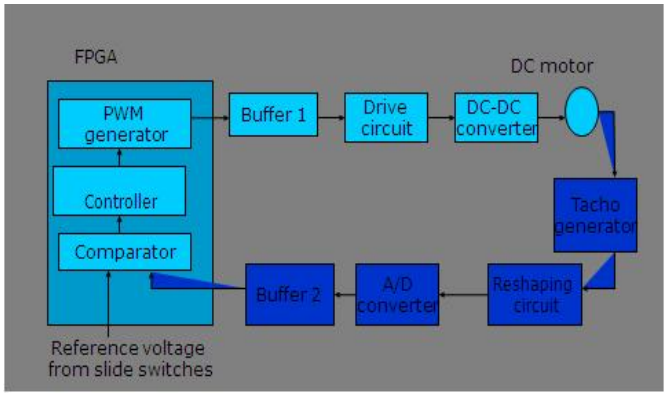


Figure (6): General block diagram for the system

In this work, a Xilinx (Spartan_3E) FPGA is used with clock frequency of (50MHz). To have a buck regulator switching frequency of about (3.051 kHz), an (14bit) up/down counter is implemented.

Figure (7) shows the result of implementation of the code in FPGA with the help of (Xilinx ISE_9.2) simulator supplied by Xilinx.

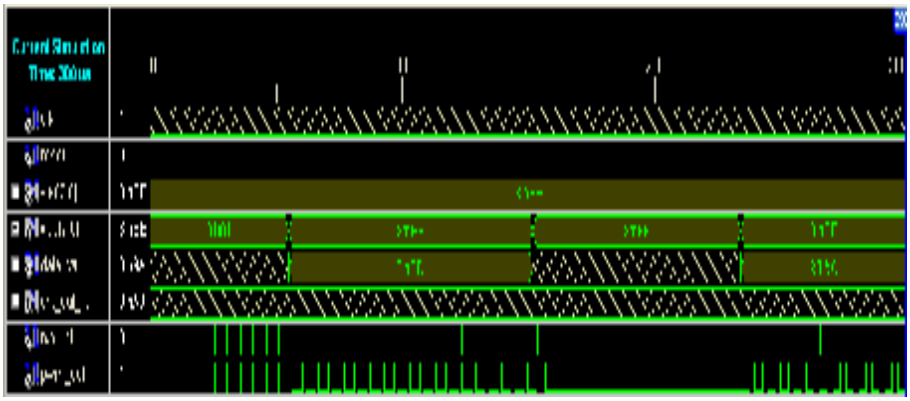


Figure (7): Simulation of the system code.

Figure (8) shows a sample of the practical PWM signal taken with (50%) duty cycle, (3.3 volt), and (3kHz frequency).

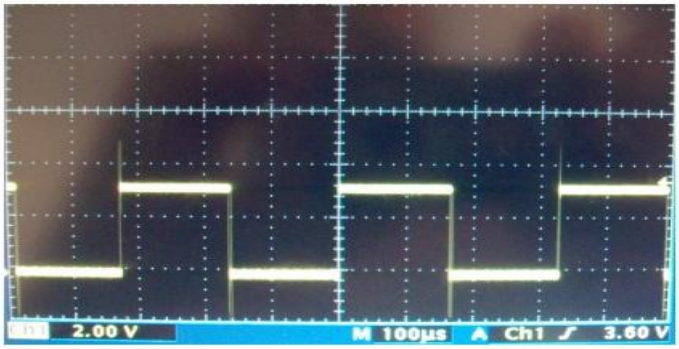


Figure (8): The PWM signal.

5. Buffer circuits:

To connect the feedback signal (ADC signal) to the FPGA and the FPGA with the driver circuit (MOSFET), buffer circuits are required. Buffer circuits are constructed around the 6N-137 optocoupler. These circuits are shown in Figures (9) and (10).

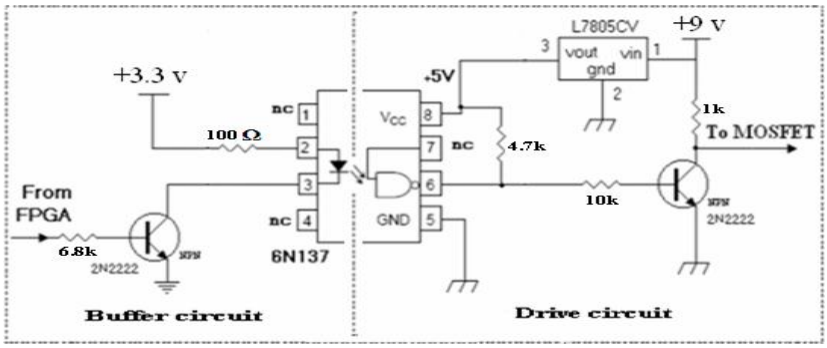


Figure (9) : Buffer-1 circuit connected between FPGA and the MOSFET

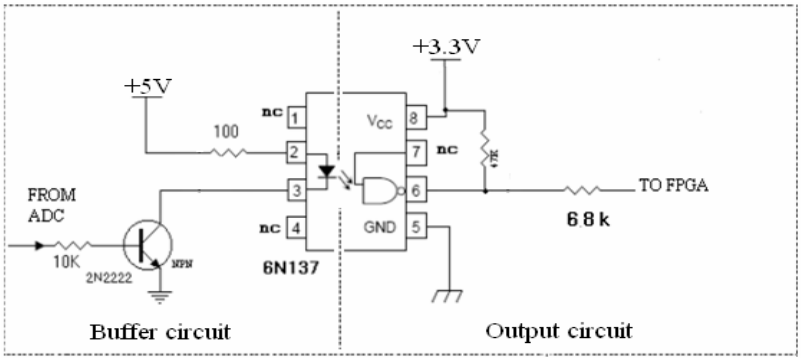


Figure (10): Buffer-2 circuit connected between ADC and FPGA

6.The MATLAB model:

When the motor parameters and the snubber circuit elements needed for the switch of the buck regulator were determined, a MATLAB model is designed by using semi power system blocks, and this model is shown in Figure (11) where it is used to check the results that have been obtained from the practical application.

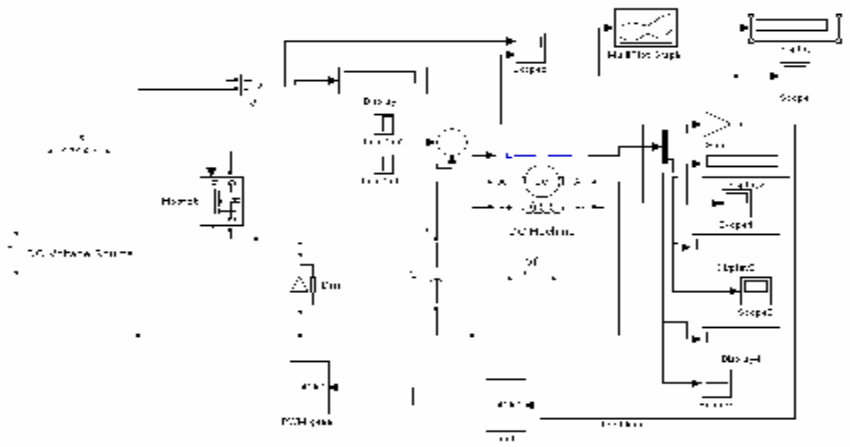


Figure (11): MATLAB model of the system

7. Practical results:

Figure (12) represents the relationship between the duty cycle and the armature voltage obtained theoreticaly and practically (open loop system).

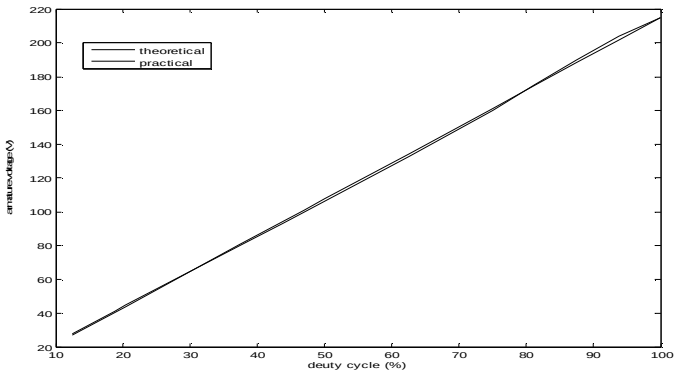
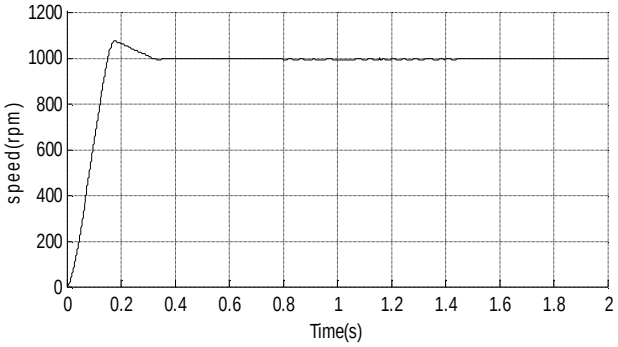
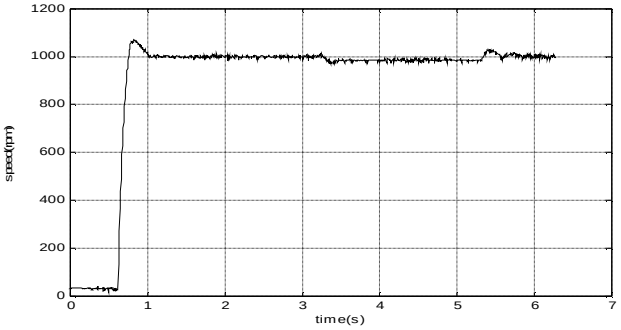


Figure (12): Relation between the duty cycle and the armature voltage

The closed loop system response is shown in Figures (13) and (14). Figure (13-a) shows MATLAB simulation at 1000 rpm with applied load 3.5 n.m, while Figure (13-b) illustrates motor speed response at 1000 rpm with applied load 3.5 n.m with steady state



(a)



(b)

Figure (13): **Dc Motor running at 1000 rpm with 3.5 n.m load**
(a) MATLAB simulation (b) Motor speed response as got by DAQ

error equals to (1.55%) as it is obtained by using a Data Acquisition Card (DAQ).

Figure (14-a) shows MATLAB simulation at 1250 rpm with applied load 5 n.m, while Figure (14-b) gives motor speed response at 1250 rpm with applied load 5 n.m and with steady state error equals to (1.44%) as it is obtained from the DAQ also.

8. Conclusions:

Acceptable results were obtained from applying the cascade compensator controller. The steady state errors were being within the limits (of 5% criteria) [7], and for both opened and closed loop control systems. The following conclusions were obtained:

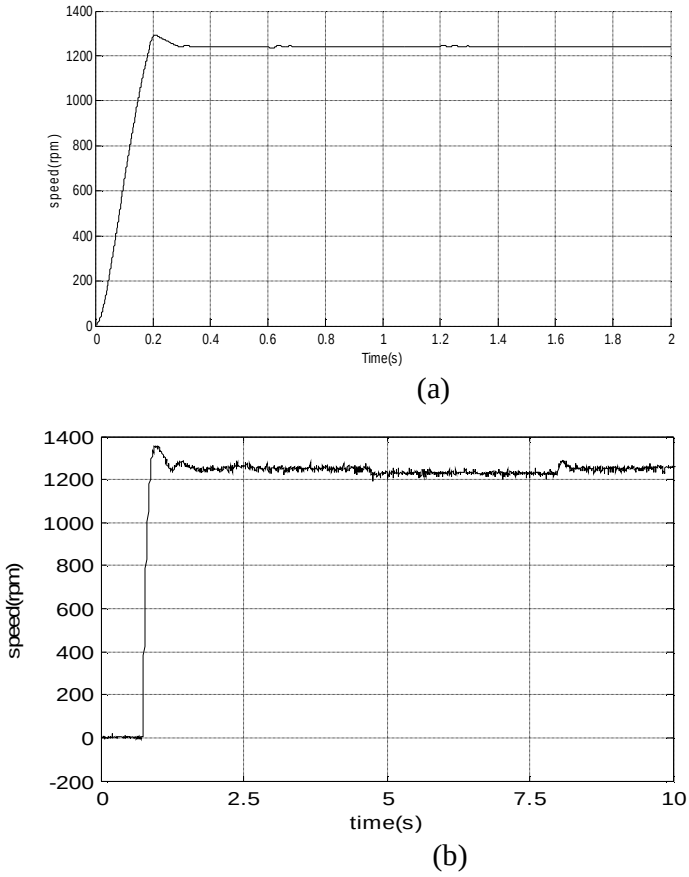


Figure (14): Dc Motor running at 1250 rpm with 5 n.m load
(a) MATLAB simulation (b) Motor speed response as got by DAQ

1-VHDL language makes the changes on the design easier to be carried out.
2- Changes on the design can be accomplished quickly and cheaply without need to change hardware components.
3- Implementation on FPGA and simulation by ISE-9.2 enabled us to check the results of the designed circuit before applying it to the motor.
4- Using the FPGA makes control of the switching frequency of the PWM output signal easier to vary; this can be accomplished by either changing the number of counter bits (n=14, in this work) or by changing the clock frequency.

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