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Simultaneous Amplitude-Modulation and Harmonic Frequency-Modulation Mode Locking of Nd:YAG Laser

Into a fundamentally AM modelocked Nd:YAG laser, we incorporate an electro-optic phase modulator driven at the 22nd harmonic (1.76 GHz). With only 0.6 Watts of RF power we obtain 17 ps pulses at 80 MHz and 8.0 Watts average optical power.

Keywords: Nd:YAG laser; Mode locking; Amplitude modulation; Frequency modulation

1. Introduction

Both AM and FM modelocking have been studied and applied extensively to many different laser systems.1;2 Analysis shows that the optical pulsewidth for either process depends on the modulation depth and frequency according to

$$\tau_p \propto \left(\frac{1}{\delta}\right)^{\frac{1}{4}} \left(\frac{1}{f_m}\right)^{\frac{1}{2}} \quad (1)$$

where _ is the modulation index and fm is the modulation frequency. Clearly, to obtain shorter pulses, raising the frequency fm provides a more rapid rate of return than increasing _. But, for lasers that are limited to constant average output power, the peak power is reduced at a rate / fm −1=2. There are many applications where this tradeo_ is undesirable (e.g. harmonic generation)

However, if two modelocking mechanisms are combined such that one operates at the fundamental frequency and one at a harmonic, the bene_ts of shorter pulses at low repetition rates will be preserved.3;4 Towards this end we report here on simultaneous modelocking; fundamental AM and harmonic FM.

We constructed an electro-optic phase modulator (FM modelocker) with a LiNbO3 crystal in a resonant microwave cavity (fm = 1:76 GHz, QL = 1500, _ = 0:59 rad=p Watt single pass).5 The modulator was placed inside an AM modelocked Nd:YAG laser (Coherent Antares), 15 cm from the output coupler. The 1.76 GHz drive signal was phaselocked to the 40 MHz acousto-optic modelocker signal. This ensured that the phase modulation was synchronized to the AM modelocker.

Simultaneous AM-harmonic FM operation was studied under constant AM modulation conditions. Fig. 1 shows the variation in pulsewidth as a function of phase modulator drive power along with a trend line denoting the −1=8 slope dependence predicted by the theory (cf. Eq. (1) and recall that _ /p Pm). At very low phase modulator drive power, laser operation is dominated by the AM modelocking mechanism. However, with remarkably low power levels, the FM modelocking process begins to dominate. With as little as 15 milliwatts (0.072 radians), the pulsewidth was halved to 40 ps. Raising the modulator power to 0.63 Watts (0.68 radians) reduced the pulsewidth to 17 ps.

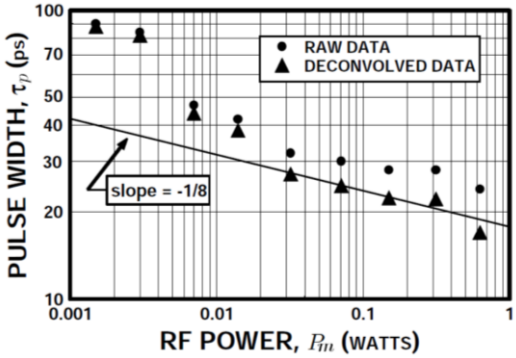

Fig. (1) Optical pulsewidth vs. phase modulator drive power (_ = 0:59 rad= p Watt single pass). Deconvolution applied to data because of photodiode's 17 ps impulse response.

Using AM modelocking alone, we routinely obtain 75 ps pulses with an average optical power of 24 Watts (_4 KW peak). With the phase modulator inserted in the cavity, the average power dropped to about 6 Watts and the laser was somewhat noisy, with occasional self-Q switching. We attribute both the loss and instability to imperfect antireflection coatings and the photorefractive effect in LiNbO3 which may be causing intensity dependent \waveguiding" and spatial mode instability. Nonetheless, we measured a \typical best" pulse of 17 ps at an average optical power of 8 Watts which corresponds to a peak power of 5.9 KW; a 47% increase.

The great utility of simultaneous fundamental and harmonic modelocking is that the pulse repetition rate remains that of the fundamental. Thus, for constant average laser power, the peak power increases linearly with the reduction in pulsewidth. Fig. 2 verifies the fundamental pulse rate when both modelockers are running. Turning o_ the AM modelocker resulted in the repetition rate rising to 1.76 GHz, as expected.

A higher temperature is desirable for the STI application, since a more dense film that is highly resistant to subsequent wet-etching steps is thus obtained. These applications are discussed in more detail later in the paper.

When tetraethylorthosilicate (TEOS) is used as the silicon source for PECVD oxide deposition, there is less cusping because of the higher surface mobility of the reactants [22]; however, a void still forms if the gap is small enough, because the conformality of the film is not 100%. This means that the amount of deposition on the sidewalls and bottom of the trench portion of a feature is less than on the top of the feature. So, in order to use PECVD films alone for gap-fill applications, they are typically used in conjunction with an argon sputter etch in a multistep PECVD-argon sputter etch-PECVD sequence described previously [23]. Conformal deposition is more typical for thermal (non-plasma) CVD processes such as low-pressure (LP) CVD at high temperatures or for ozone-TEOS atmospheric or subatmospheric pressure (AP or SA) CVD at lower temperatures (less than 600°C). Furthermore, HDP CVD results in a completely different type of profile because of the "bottom-up" deposition from the simultaneous deposition and etching. The resultant topography from any of these CVD processes plays a decisive role in the choice of subsequent planarization techniques. TEOS was the silicon source for the PECVD and the SACVD, and silane for HDP CVD. The typical "bread-loaf" profile of the PECVD oxide film can be adjusted by varying process parameters such as temperature, pressure, and silicon source. The profile of the SACVD oxide film is conformal, and the unique profile of the HDP CVD oxide film is a result of simultaneous etching and deposition. Note that SACVD is a non-plasma process.

Typically, thermal CVD processes such as LPCVD BPSG, APCVD (or SACVD) BPSG, or PSG are used to passivate the polysilicon/metal silicide gate conductor for sub-half-micron devices because of their high-aspect-ratio fill capability compared to plasma CVD processes and because there are no plasma damage concerns with thermal CVD processing. Process-induced IC device damage from plasma processing (in particular at the gate-conductor level, because there is no device protection) is a critical issue for the PECVD passivation dielectrics. Briefly, low process pressure during deposition of the PECVD PSG was identified as the main factor causing gate-oxide charge damage. Increasing the pressure for the PECVD PSG process regardless of dopant source (trimethylphosphite or triethylphosphate) resulted in no charge damage on antenna test sites and device structures. A more recent study describes another technique used to optimize a PECVD PSG process for plasma damage designated as corona oxide semiconductor (COS) charge measurement [24]. The technique, combined with the antenna test structure method of measuring plasma damage, provides a fast and cost-effective way to optimize plasma CVD processes.

Doped silicon oxide films such as PSG or BPSG are preferred for gate-conductor passivation because of their mobile ion barrier properties [25], low reflow temperature for local planarization (applies to BPSG only), high etch selectivity to the underlying barrier layer (e.g., nitride [26]), and faster polishing rate compared to undoped silicon oxide. In this paper, we discuss our recent work with HDP CVD PSG including gap-fill and plasma damage results. We have previously published an overview of our own work and that of others in IBM on relevant thermal CVD processes and applications [27].

The gap-fill requirement for dielectrics in the "back-end-of-line" (BEOL) depends on the interconnect fabrication methods used. Multilevel interconnects usually involve two types of planarization methods: the planarization of interlayer dielectrics and the planarization of metal layers. For the former, for example, an Al(Cu)-based layer is patterned into lines and the insulator is deposited between the spaces and above the lines. Therefore, a critical requirement in this case is the filling of the gaps between the lines without void formation. Void-free filling of high-aspect-ratio features is not a simple matter and requires the use of advanced insulator deposition processes such as HDP CVD. For submicron metal interconnect fabrication, the insulator deposition is generally followed by partial planarization using spin-on-glass (SOG) [28], a resist etch-back [29], or a global planarization using, for example, chemical-mechanical polishing (CMP). For the planarization of metal layers, the damascene technique is most commonly used; several papers reporting its use in IBM have been published [30]. Using this technique, a dielectric such as silicon oxide is deposited on a planar surface and the wiring level is patterned into the dielectric using photolithography and RIE. A thin metal liner and a metal such as tungsten (or aluminum or copper) are then deposited on the patterned dielectric and subsequently planarized by CMP, stopping on the dielectric and leaving metal in the patterned features. Therefore, in the damascene technique, the metal rather than the insulator must fill the high-aspect-ratio features.

A critical film parameter for both interconnect fabrication techniques is the

dielectric constant (k) of the IMD material. Use of a material having a lower dielectric constant leads to lower total capacitance, decreasing the interconnection delay and power dissipation [31], and thus enhancing performance. To achieve long-range interconnection performance objectives, low-dielectric-constant IMD will be required [32]. The dielectric constant of PECVD silicon oxide is typically 4.1-4.2. By doping the oxide with fluorine, the dielectric constant can be reduced to 3.0-3.7, depending on the fluorine concentration [33]. Si-F replaces the Si-OH and Si-H bonds in the oxide; since fluorine is more electronegative, the polarization changes, lowering the dielectric constant. SOG dielectrics (siloxanes, silsesquioxanes) and organic polymers formed by spin coating (polyimides, fluorinated polyimides, bisbenzocyclobutenes), poly(arylethers), or vapor-phase deposition (parylene N, parylene F, teflon) provide dielectric constants in the range of 1.9-3.0 [34]. Most polymers with a dielectric constant less than 3 are stable to only about 350°C. However, a recent publication on laser-evaporated siloxane thin films reports a dielectric constant of 2.0 and thermal stability to 400°C, although integration results were not published [35]. Also, it has been reported that parylene exhibits a high thermal stability [36], and its successful integration into a metal RIE BEOL has been demonstrated [37]. However, damascene integration may be more difficult to achieve because of the softness of parylene films. Spun-on films of materials such as nanoporous silica and xerogels exhibit a higher thermal stability and low dielectric constants (1.3-2.5), depending on their porosity [38], but associated process integration is challenging. There has been increased development activity in plasma-assisted CVD of amorphous carbon and fluorinated carbon films because of their low dielectric constants (2.3-2.7) and thermal stability up to 400°C [39]. Relevant work on insulators having low dielectric constants has been described elsewhere [40].

In this paper, the plasma-assisted CVD of low-dielectric-constant insulators of potential interest at the ULSI level, including fluorine-doped silicon oxide and amorphous carbon and fluorocarbon, was discussed. To be suitable for the deposition of such insulators, plasma-assisted CVD should be applicable at relatively low substrate temperatures, should not damage underlying layers or devices that may be present on the substrate during deposition, and should produce insulators which, in addition to having low dielectric constants, satisfy etching, annealing, planarization, and stability requirements.

2. Fundamentals of PECVD

In thermal CVD, gas-phase reactive species are generated by heating of initial reactants. In plasma CVD, the plasma energy supplied by an external rf source takes the place of the heating to generate the species that subsequently react and deposit on substrate surfaces. Significantly, excessive heating and degradation on the substrate can be avoided by using plasma electron kinetic energy instead of thermal energy. Besides the aspect of generating reactive species at much lower processing temperatures compared to conventional CVD processing, the ion bombardment can be used to modify film characteristics. Plasma CVD processes can be classified into many sub-processes, such as plasma evaporation deposition, plasma sputtering deposition, plasma ion plating, and plasma nitriding. This classification depends on the conditions of the plasma generated, configuration of the vacuum system, location of the substrate, and type of power supply [19-21]. Plasma-assisted CVD processes for semiconductor processing are generally carried out at pressures of 1mTorr to 20Torr substrate temperatures in the range of 100 to 500°C, rf power densities <0.5 W-cm^{-2}, electron densities of 1.0 x 10^{8} to 1.0x10^{12}cm^{-3}, electron mean free paths of <0.1 cm, and average electron energies of 1eV to 6eV.

When the plasma initiates, energy from the rf electric field is coupled into the reactant gases via the kinetic energy of a few free electrons. These electrons gain energy rapidly through the electric field and lose energy slowly through elastic collisions. The high-energy electrons are capable of inelastic collisions that cause the reactant gas molecules to dissociate and ionize, producing secondary electrons by various electron-impact reactions. Table (1) lists typical electron-impact reactions of silane molecules in an rf plasma discharge. In a steady-state discharge, the electrons generated by electron-impact reactions equal those electrons that are lost to the electrode, walls, and reactive species by attachment and recombination reactions [1].

The two important aspects of a plasma glow discharge are the nonequilibrium low-temperature gas-phase chemical reactions that generate radical and ion reactive species in the plasma discharge, and the flux and energy of these reactive species as they reach and strike the surface of the film being deposited. The bombardment of the ionic species on the surface of the film, which controls the surface mobility of the precursor, is the predominant factor in determining film composition, density, stress, and step coverage or conformality at the relatively low temperatures used in plasma CVD. Reactant gases similar to those used for

thermal CVD processes are used for plasma CVD to deposit silicon-based dielectrics at lower deposition temperatures.

Table (1) Typical electron-impact reactions of silane molecules in an rf plasma discharge. The asterisk (*) refers to electronic excited state [1]

Reactant	Reaction products	Enthalpy of formation (eV)
$e^- + SiH_4 \rightarrow$	$SiH_2 + H_2 + e^-$	2.2
	$SiH_3 + H + e^-$	4.0
	$Si + 2H_2 + e^-$	4.2
	$SiH + H_2 + H + e^-$	5.7
	$SiH^* + H_2 + H + e^-$	8.9
	$Si^* + 2H_2 + e^-$	9.5
	$SiH_2 + 2H_2 + 2\ e^-$	11.9
	$SiH_3 + H + 2\ e^-$	12.3
	$Si + 2H_2 + 2\ e^-$	13.6
	$SiH + H_2 + H + e^-$	15.3

2.1 Reaction kinetics

Reactions during plasma deposition are complex and not completely understood. Elementary reactions that occur in plasma have been discussed by various authors [41-43]. The initial reaction between electrons and reactant gas molecules or between reactant gas molecules in plasma can be classified as elastic or inelastic. In the elastic collisions, only minimal translational energy transfer occurs between the gas molecules and reactant gases. For plasma processing, the elastic collisions play a less important role in reactant dissociation. Significantly more translational, rotational, vibrational, and electronically excitational energy transfer occurs in the inelastic collisions. The major inelastic reactions among electrons, reactant gases, and surface that occur during plasma-assisted CVD processing are typically represented in Tables (2-4).

Table (2) Initial electron-impact reactions [1]

Excitation (rotational, vibrational, and electronic)	$e^- + A_2 \rightarrow A_2 + e^-$
Dissociative attachment	$e^- + A_2 \rightarrow A^- + A+ + e^-$
Dissociation	$e^- + A_2 \rightarrow 2A \bullet + e^-$
Ionization	$e^- + A_2 \rightarrow A_2+ + 2e^-$
Dissociative ionization	$e^- + A_2 \rightarrow A+ + A + 2e^-$

Some of the inelastic collisions between inert gases and reactants (such as helium or argon with silane) significantly affect the chemical nature of the discharge and the properties of the deposited films [44-46]. In many plasma deposition processes, inert carrier and diluent gases such as helium and argon have been used to form "cooler" plasma, to create more controlled reaction pathways via Penning reactions between carrier and reactant gases [47], and to suppress gas-phase reactions between reactive species. As a result, a plasma diluted with inert gases such as helium can be used to deposit higher-quality insulators.

Table (3) Inelastic reactions among reactants, inert gases, and substrate. M refers to the inert gas or substrate, and A, B, and C refer to the reactant gases [1]

A	
Penning dissociation	$M^* + A_2 \rightarrow 2A \bullet + M$
Penning ionization	$M^* + A_2 \rightarrow A_2^+ + M + e^-$
Ion-ion recombination	$M^- + A_2^+ \rightarrow A_2 + M$
	or
	$M^- + A_2^+ \rightarrow 2A \bullet + M$
Electron-ion recombination	$e^- + A_2^+ \rightarrow 2A \bullet$
	$e^- + A_2^+ + M \rightarrow A_2 + M$
Charge transfer	$M^+ + A_2 \rightarrow A_2^+ + M$
	$M^- + A_2 \rightarrow A_2^- + M$
B	
Collisional detachment	$M^* + A_2^- \rightarrow A_2 + M + e^-$
Associative detachment	$A^- + A \rightarrow A_2 + e^-$
Atom recombination	$2A + M \rightarrow A_2 + M$
Atom abstraction	$A + BC \rightarrow AB + C$
Atom addition	$A + BC + M \rightarrow ABC + M$

Table (4) Heterogeneous reactions between plasma and surface. S refers to the surface in contact with the plasma, and A and B refer to the reactant gases [1]

Atom recombination	$S - A + A \rightarrow S + A_2$
Metastable de-excitation	$S + M^* \rightarrow S + M$
Atom abstraction	$S - B + A \rightarrow S + AB$
Sputtering	$S - B + M^+ \rightarrow S^+ + B + M$
Surface contact ionization	$S + B^* \rightarrow B^+ + e^- + S$

2.2 Deposition Mechanisms

One of the major advantages of plasma deposition processing is its flexibility for depositing films with desirable properties. For conventional thermal CVD processing, physical and chemical properties of the deposited film pertaining to its stress, conformality, density, moisture resistance, and gap-fill properties can be altered by changing the composition and/or type of reactive species. In plasma-assisted CVD, this can be accomplished by varying deposition parameters such as temperature, rf power, pressure, reactant gas mixture ratio, and type of reactant. For example, silicon oxide films deposited with TEOS generally show higher step coverage or conformality than those deposited

with silane in a plasma-assisted CVD process. For plasma-assisted CVD of silicon oxide films, properties can be modified not only by changing the type of reactive species, but also by the extent of ion bombardment.

In general, the deposition mechanisms for a plasma CVD process can be qualitatively divided into four major steps, as shown in Fig. (1). Step 1 includes the primary initial electron-impact reactions between electron and reactant gases to form ions and radical reactive species (Tables 1 and 2). Next, in step 2, transport of these reactive species occurs from the plasma to the substrate surface concurrently with the occurrence of many elastic and inelastic collisions in both the plasma and sheath regions, classified as ion and radical generation steps [48]. Step 3 is the absorption and/or reaction of reactive species (radical absorption and ion incorporation) onto the substrate surface. Finally, in step 4, the reactive species and/or reaction products incorporate into the deposited films or re-emit from surface back to the gas phase. Because of their complexity, the latter two steps are the least known and least studied aspects of plasma CVD. Significant roles are played by ion bombardment [49] and various heterogeneous reactions between ions and radicals with the depositing surface in the sheath region. The two steps critically affect film properties such as conformality [50], density, stress [51], and "impurity" incorporation.

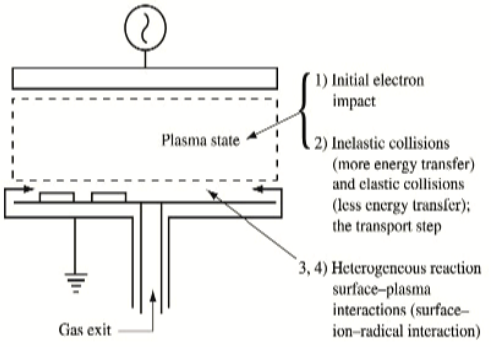

Fig. (1) Four steps that characterize the mechanisms of plasma CVD process [1]

Plasma CVD of amorphous and microcrystalline silicon are the most studied plasma CVD processes, with hundreds of publications on their deposition kinetics and mechanisms. The basic gas-phase chemistry of the silane plasma has been studied by various techniques [49-52]. Different mechanisms have been suggested for the dominant reaction pathway of silicon deposition. One mechanism describes SiH_3 (silyl) radicals playing a dominant role [53], while others describe the decomposition of silane to SiH_2 (silylene) and then SiH_2 insertion into gas-phase SiH_4 to form higher silane species [54] as the main silicon deposition mechanism.

4. Conclusions

We have reviewed the plasma-assisted CVD of dielectric films, with an emphasis on aspects relevant to ULSI semiconductor circuits. In addition, we have indicated that manufacturing needs must be considered early in the process and tool development phase. Obviously, the ultimate goal is to optimize a plasma CVD process for a particular application at the lowest cost of ownership. Future research and development must focus not only on specific technical issues that arise with each new IC generation (such as integration of a stable low-*k* IMD into the BEOL), but also on manufacturability and cost. With 300mm-diameter wafers containing sub-0.25µm semiconductor IC circuits on the horizon, the technical and manufacturing issues are daunting; new challenges are presented to both the semiconductor manufacturers and their equipment suppliers, even for the conventional processes used in IC production.

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