THE INFLUENCE OF HEATING TREATMENT ON PHYSICAL PROPERTIES OF POROUS SILICON

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Abstract:

In this work we studying the effect of thermal treatment on the electrical and conduction properties of metal /porous silica /n-si /metal prepared by photo electro chemical etching for etching time (15 min. Oxidation occur in oxidation time (15-150)sec at 750Ċ.After investigated current–voltage (J-V)measurement we found increase in rectification ratio ,barrier height increase with oxidation time, the rectification ration was 5 before oxidation will be 21 after 30 s oxidation time, barrier height value was (0.756eV) will be(0.85eV) at oxidation time 30 s ,the ideality factor after oxidation was 15 will be 2.75 at 30 sec of oxidation time mean that the device approach from the ideality characteristics.

Keywords: Porous Silicon, photo electrochemical ,rapid thermal oxidation.

Introduction

Since canham [1]demonstrated visible light photoluminescence(PL) from Porous silicon (PSi),much effort has been focused on the possibility of producing optoelectronic devices by using this new material . Sio_2/PSi systems are different in their electrical properties compare with silicon dioxide and silica[2] .Electro luminescence (EL)is also observed from schottky diodes formed form PSi under forward bias [3] it is important to study the influence of recombination center surface state and electrical contacts on the OPS (oxide porous silicon)and electrical properties for this purpose much attention is being paid to study the electrical properties of PSi-based structure .for most of the previous work ,the rectification ratio in (J-V)curves is interpret in terms of the existence of shottky barriers between the metal /porous silica interface [4].the research [5] believe that the metal/psi junction is not as shottky barriers but forms a non-ideal ohmic contact. the aim of this paper is to investigate the effect of oxidation time on the electrical properties like ,rectification ratio, barrier height ,resistivity and ideality factor on transport mechanism for porous silicon. The purpose of utilize rapid thermal oxidation is to obtaina partially oxidized not fully oxidized.

Expeirmental work

Porous silicon samples were prepares by photo electrochemical etching of (111) n-type silicon substrates with resistivity (3.5Ω.cm) in (1:1) solution of (HF) acid (47%)and ethanol at current density (20mA/cm^2) for (15min).The wafer has been cut out into small fragments in dimensions of(1.5×1)cm ,these pieces were rinsed with ethanol to remove dirt followed by etching in dilute (10%)hydrofluoric (HF)acid to remove native oxide layer flowed by rinsed by ethanol after that leave it to dry and consumed in container fully by ethanol to prevent it to oxide. the simple set –up of PEC etching process consisted of one commercially available CW diode laser with power (2W) and (810nm) wave length .the photo–electrochemically etched area for all samples has been (0.5cm^2) .Fig. (1) depicts a schematic diagram of the PEC set-up .

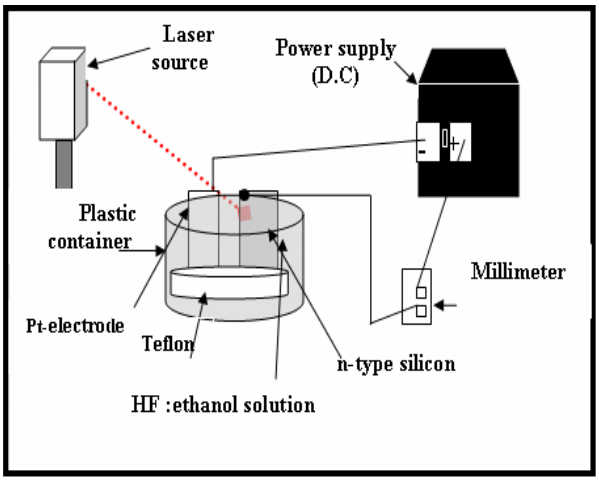

Fig. (1) : Schematic digram depicts the PEC proces.

The thermal oxidation occur at (750◦C) by using tungsten halogen lamp (OSRAM 64575) with (1000 W) power for different

oxidation times(15-150sec) in O_2 atmosphere, to form a thin$Sio_{2\ -\ layer}$ above the porous silicon Fig.(2) show the RTO System.

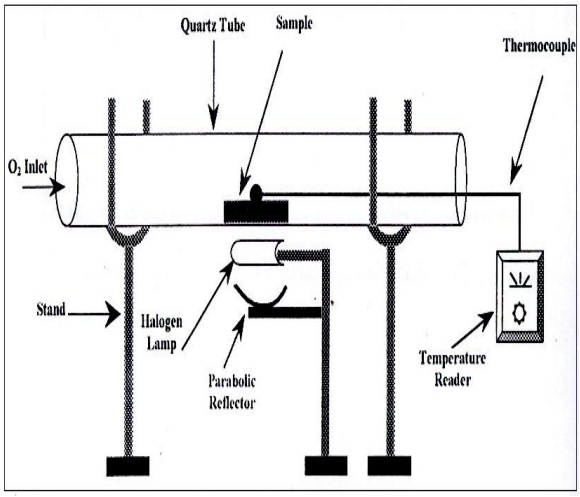

Fig. (2) : shows the manufactured system of rapid thermal oxidation.

The structure of the MOS photo detector is Al $_{(thin)}$/porous silica /n-Si/$AL_{(ohmic)}$ was achieved by thermal evaporation technique. Al films was used to create an intimate backside contact the metal spot was performed on porous region to prevent direct contact between the silicon and the metal.

Result and Dscussion

Fig. (3) show the calibration settings of the pyrometer were determined in dummy runs by calibration with thermocouple directly attached to a silicon wafer at temperature 750 ^{o}C.

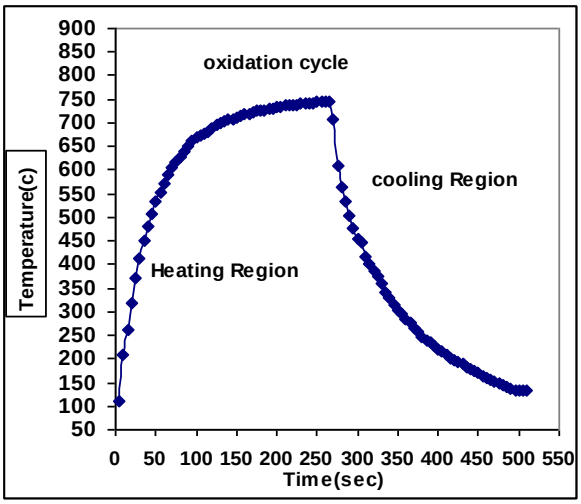

Fig. (3) : Shown the characteristics of RTO system.

Where its appear from figure three regains [heating reign, equilibrium reign (oxidation region) and cooling reign] which responsible for oxidation stability obtained by calibration by using thermocable with reader K-type, Fig.(4)show the electrical behavior, J-V characteristics of Al/porous silica/Si/Al sandwich structure.

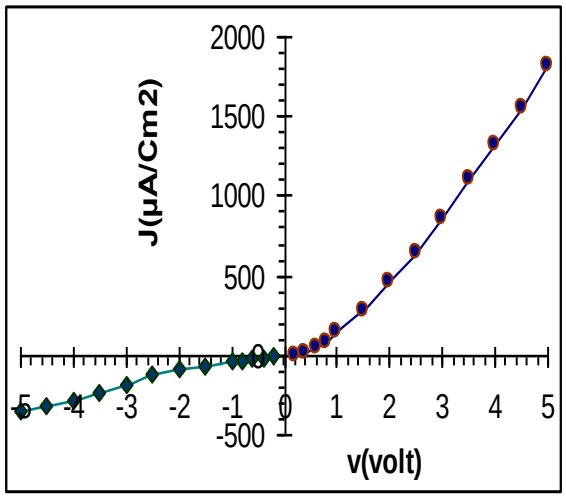

Fig. (4) : The J-V characteristics of as prepared psi.

which is contains PSi such as shottky diode generally is determine by depending on the characteristics of current-voltage curves[1].

The J-V characteristics occur under dark and at room temperature of the Al/PSi/n-Si/Al sandwich structure include PSi layer prepared at an etching time (15 min)show rectifying behavior and double current saturation .We have attributed these result to silicon/porous silicon hetrojunction act as double –shottky –diode [5] .

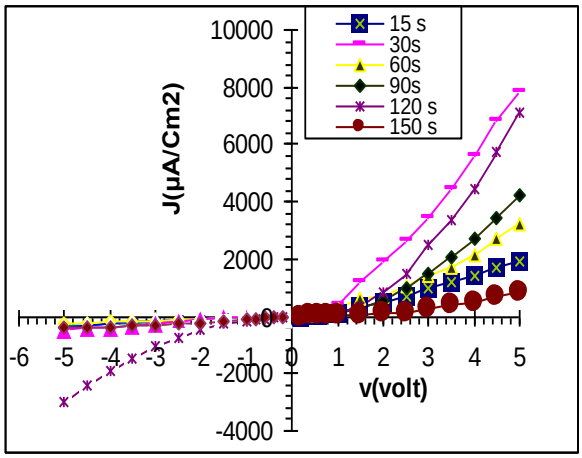

Fig.(5) : The J-V characteristics of the junction .

From Fig.(5) we can show that the reverse current will be decreased and forward current increased rather than as prepared Fig.(4) that mean the rectifying behavior increased after oxidation due to the heterojunction potential barrier at the oxide /PSi interface that attributed to the quantum confinement in silicon nano crystallites [6].

Fig.(6) show the rectifying characteristics obtained at 5 volt. rectification ratio meaning the ratio between forward current to the reverse Current, it for as prepared was equal to 5 ,With increase oxidation time the rectification ratio increase and reach to optimum value about 21 at oxidation time (30 sec).

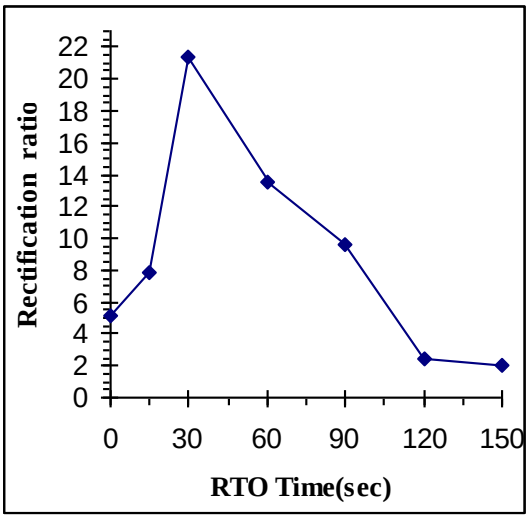

Fig. (6) : Show rectification ratio versus oxidation time.

this increased in rectification factor is attributed to the formation a thin oxide layer between AL metal and Si [7] also attributed to formation of an isotope heteojunction ,after that time the rectification ratio will be decreased is due to the defect formed by the sympathize silicon-oxygen structure in a very thin oxide layer and they would act as tunneling center, for oxidation time is longer than (30 sec) the oxide layer is thicker the tunneling probability of photo carriers and the thermal generated carriers through the oxide layer are reduced and hence the dark current to reduced [8]. The oxide thickness is estimated by using equation for high resistivity n-type for silicon [9].

$R_\circ = 1.8\times10^{5} \exp(-1.21/KT)$ Å/sec .....(1)

where $R_\circ$ is the oxidation rate Å/s ,1.21eV is the activation energy required to diffuse oxygen inter silicon for rapid thermal oxidation and it is equal to 2 eV for Deal –Grove model (classical dry oxidation, the oxide thickness which obtain in bytherotical equation (1) is illustrated in Fig. (7).

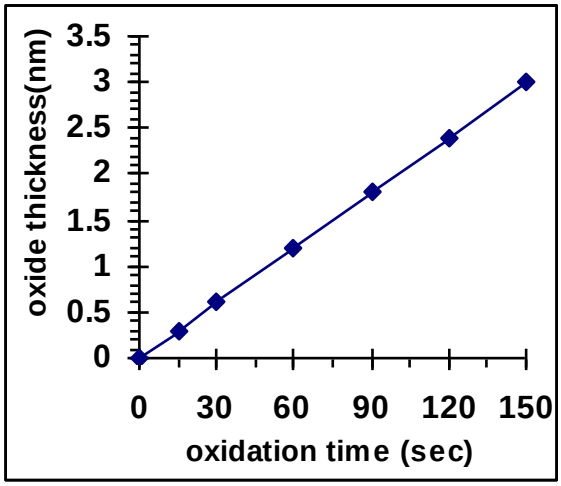

Fig. (7) : The oxide thickness at deferent oxidation time.

The typical of the measured J-V is very similar to shottky diode characteristics and may analyzed by using the following equation which described by :

$$J = J_s[\exp\left[\frac{qv}{nkT}\right]-1] \quad \text{.....(2)[10]}$$

Where Js: is the saturation current density obtained from semi-log forward bias, k :Boltzman constant (J/K), T: room temperature (K), q: electron charge in C and n: ideality factor is given by [10]:

$$n = \frac{q}{kT}\frac{\partial v}{\partial \ln J} \quad \text{.....(3)}$$

Fig.(8) show the changing in ideality factor with oxidation time .

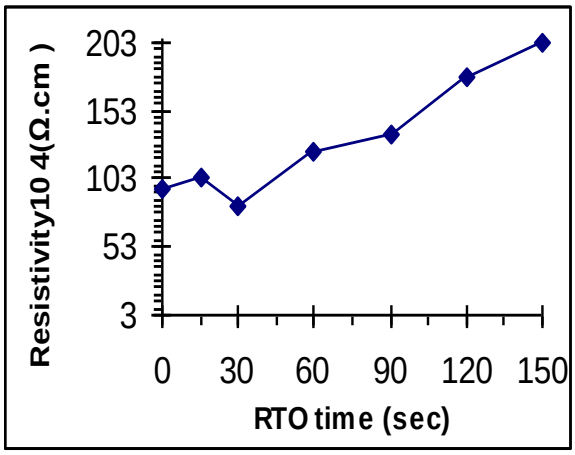

Fig.(8)the ideality factor for as prepared and at different oxidation time.

The ideality factor decreased with oxidation time, that mean approach devise from the ideality characteristics after (60 sec) it is come back to increased with oxidation time because the surface channel is present in our diodes[12],see Table (1).

Table (1)
Show the electrical value for different oxidation time.

Oxidation time (sec)	Rectification ratio	Saturation current density ($\mu A/cm^2$)	Ideality factor(n)	Resistivity ($\Omega.cm)*10^4$	Barrier height (eV)
0(as prepared)	5.144969	1	15.82	96	0.756
15	7.803571	0.25	10.47	103	0.81
30	21.42077	0.05	2.75	84	0.8515
60	13.51351	0.9	6.43	123	0.7769
90	9.578947	1.1	6.66	136	0.7718
120	2.390057	1.3	5.77	178	0.767
150	1.992883	1.5	8.248	202	0.7638

We can also calculate the resistivity for PSi after and before thermal oxidation from J-V curve, Fig.(9) show the behavior of resistivity with oxidation time .

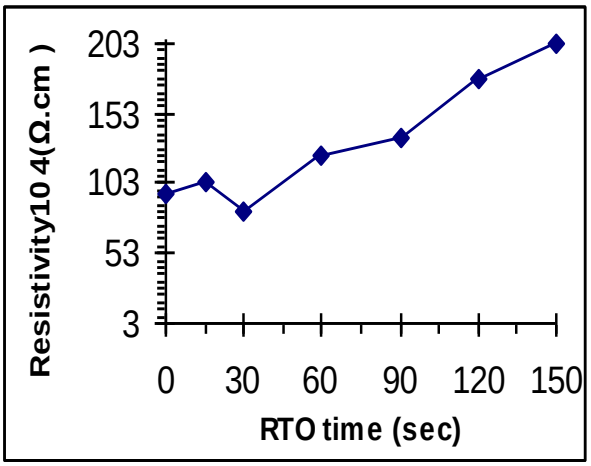

Fig. (9) : The resistivity with oxidation time.

We can from Fig.(9) observed that at the beginning from oxidation time the resistivity decreased is due to PSi layer have a very large effective surface area and has a large of dangling bonds after oxidation the dangling bond is replaced by oxygen bonds that mean oxidation decrease the defect surface and increased current density [6] sub sequent resistively will be decrease, with increase oxidation time resistivity come back to increase , that is due to with increase oxidation time the porous depth will be increased [13] which making to increase resistance according to relations [11]:

$R=\rho . d/A$ ..... (4)[11]

Where R: resistance (Ω), ρ:resistivity (Ω. cm), A: sample area(cm^2),d:porous layer thickness(cm), figure(10) show the barrier height was found increased with oxidation time and have maximum value at oxidation time (30sec)about(0.836 eV).

We can calculate the barrier height from (Js) saturation current density [15].

$JS=A^{**}T^2 \exp[q \Phi Bn /KT]$ .....(5)

Where A**:is the effective Richardson Which equal to 120 ($A/K^2.cm^2$)for n-type, from equation the barrier height is equal to

$\Phi Bn=kT/q \ Ln \ A^{**}T^2/JS$ ..... (6) [5]

Fig. (10) show that the barrier height increase with oxidation time.

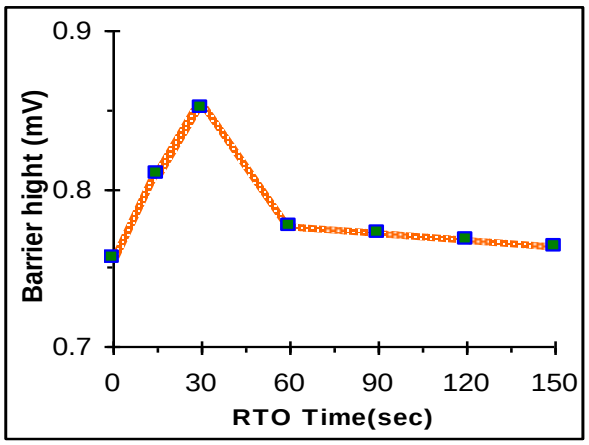

Fig.(10): The barrier height with oxidation time.

The barrier height reach to optimum value at 30 sec the increasing in value of barrier height that because the addition in potential height due to the oxide layer according to the relation[13]

$\Phi ms = kT/q \; Ln \; A \; T^2/Js + kT/q \; \chi^{1/2} \; \delta$

.....(7) [13]

The equation (6) can be written as

$\Phi ms = \Phi Bn + (kT/q) \; \chi^{1/2} \; \delta$..... (8)[14]

Where χ :is average barrier height(eV), δ :the oxide thickness, this equation represent the effective barrier height for metal /oxide/semiconductor contact .The barrier height in MOS porous silicon represent the summation for shottcky barrier and barrier high for the oxide layer ,The oxide making to decrease the (pinning) trapping charge which caused to decrease the barrier height in the contacts region, If the pinning stale in the PSi surface make to decrease the potential at the contact area. The decreasing in barrier high after (30 sec) of oxidation is due to the defects concentration in the oxide layer is presented by (oxidation) and the interface capture (SiO_2/PS/Si).Although, the little value of barrier high after that time of oxidation the barrier high potentional is still larger than metal/PSi structure before oxidation treatment . The surface of silicon is usually due to the presence the native oxide layer it is expected that PSi is depleted and it extends over a distance of a few tenth of microns after oxidation. the depth of depletion depends on carrier concentration and the surface charge of silicon [14].

Conclusion

Sio_2/PS layer in this study formed by using Rapid thermal oxidation process in atmosphere ,ideality factor, rectification ratio ,barrier height and resistivity were measured at different oxidation time (15-150) sec at temperature 750 ^oC .we will observed the barrier the rectification ration was 5 before oxidation will be 21 after 30 s oxidation time ,barrier height value was (0.756eV) will be (0.85eV) at oxidation time 30 s ,the ideality factor after oxidation was 15 will be 2.75 at 30 sec of oxidation time after this time the barrier height and rectification ratio begin to decrease because the increase oxide layer thickness working to consume column by growth with in PSi layer production increase energy gap and making to porous Asilicon to be behavior like insulator, the resistivity increased with oxidation time due to increase porous silicon thickness after thermaloxidation.

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الخلاصة

في هذا البحث تم دراسة تأثير المعالجة الحرارية السريعة على الخصائص الكهربائية وميكانيكية التوصيل للسليكون المسامي المحضر بطريقة تشعيع الليزر أثناء عملية القشط الكهروكيميائي بزمن (١٥ دقيقة) عملية الأكسدة جرت بزمن (١٥-١٥٠ ثانية) عند درجة حرارة (٧٥٠Ċ) من خلال دراسة الخصائص الكهربائية أن نسبة التقويم و حاجز الجهد تزداد بزيادة زمن الأكسدة الحرارية الأكسدة الحرارية . قيمة حاجز الجهد كانت(eV ٠.٧٥٦) أصبحت (eV ٠.٨٥) عند زمن أكسدة ٣٠ ثانية،عامل المثالية وجد انه قبل عملية الأكسدة ١٥اصبحت قيمته ٢.٧٥ عند زمن الأكسدة ٣٠ ثانية مما يعني اقتراب الجهاز من الخصائص المثالية.