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Stress Management and Interfacial Strength of Gallium Nitride Layer Grown on Diamond Substrate

In this work, the stress management and interfacial strength of gallium nitride layer grown on diamond substrate, as well as homogeneous interfacial thermal properties across the wafer, have been achieved. These results on such material systems are highly important for reliable high-power electronics based on this material system, such as high electron mobility transistors.

Keywords: GaN; Stress management; Interfacial strength; Wafer mapping
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Introduction

A high-electron-mobility transistor (HEMT), also known as heterostructure FET (HFET) or modulation-doped FET (MODFET), is a field-effect transistor incorporating a junction between two materials with different band gaps (i.e. a heterojunction) as the channel instead of a doped region (as is generally the case for MOSFET). A commonly used material combination is GaAs with AlGaAs, though there is wide variation, dependent on the application of the device. Figure (1) shows the cross section of a GaAs/AlGaAs/InGaAs pHEMT.

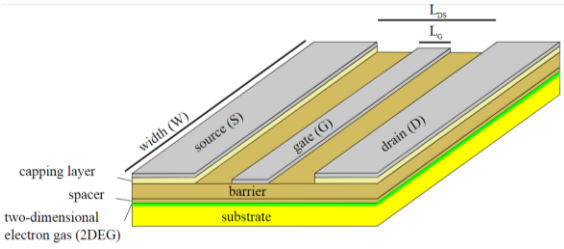

Fig. (1) Cross section of a GaAs/AlGaAs/InGaAs pHEMT

Devices incorporating more indium generally show better high-frequency performance, while in recent years, gallium nitride HEMTs have attracted attention due to their high-power performance. Like other FETs, HEMTs are used in integrated circuits as digital on-off switches. FETs can also be used as amplifiers for large amounts of current using a small voltage as a control signal. Both of these uses are made possible by the FET's unique current-voltage characteristics. HEMT transistors are able to operate at higher frequencies than ordinary transistors, up to millimeter wave frequencies, and are used in high-frequency products such as cell phones, satellite television receivers, voltage converters, and radar equipment. They are widely used in satellite receivers, in low power amplifiers and in the defense industry. Figure (2) the band diagram of GaAs/AlGaAs heterojunction-based HEMT, at equilibrium.

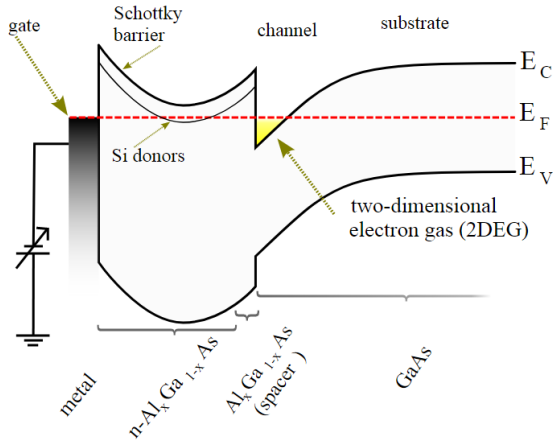

Fig. (2) Band diagram of GaAs/AlGaAs heterojunction-based HEMT, at equilibrium

Significant efforts and progress has been made to integrate diamond with "III-V"-based electronics for improved thermal management. Currently, many "III-V"-on-diamond high electron mobility transistors (HEMTs) have been demonstrated with outstanding performance for high-power microwave device applications [1,2]. The Element-Six approach as one of the various GaN-diamond integration technologies is considered in this work. It involves removing the substrate from a standard GaN-on-Si wafer, followed by the deposition of a thin dielectric layer and the subsequent growth of chemical-vapor deposited (CVD) diamond on the exposed GaN surface. Stress management in the GaN and the mechanical stability of the GaN-diamond interface, owing to the large thermal expansion mismatch between these materials, is naturally a concern which arises. Moreover, the wafer-level homogeneity of mechanical and thermal properties is yet to be assessed.

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In this paper, we use Raman spectroscopy to characterize the GaN layer stress in the manufactured GaN-on-diamond wafers, showing that this stress has nearly been eliminated through successive generations of wafer development. Using a micro-pillar based fracture test, we illustrate that the GaN-diamond interface has excellent mechanical stability. We further demonstrate a nearly homogeneous distribution of the effective thermal boundary resistance (TBR_{eff}) between GaN and diamond across a three-inch wafer using transient thermoreflectance mapping.

Measurement Technique

Raman spectroscopy measurements were performed using a Renishaw InVia system with a 488 nm Argon laser. The E_2 peak with stress coefficient -2.7 cm^{-1}/GPa [3] was used to determine the inbuilt stress in the GaN layer, referenced to a stress-free value of 567 cm^{-1} measured for bulk GaN (consistent with previously reported values).

To assess the GaN-diamond interfacial strength, micro-pillars comprising the layer structure of GaN/dielectric/diamond were created using focused Ga^+ beam milling. A force measurement silicon probe mounted on a micro-manipulator was used to apply controlled displacement or load to the GaN layer from the side of the micro-pillar. The force was measured by a piezoelectric sensor with a resolution of 0.1 μN. The deformation and the fracture process were monitored *in situ* in a scanning electron microscope (SEM).

The TBR_{eff} at the GaN-diamond interface is a lumped thermal resistance with contributions from the amorphous dielectric layer with its lower thermal conductivity and the diamond nucleation layer formed in the initial phases of the diamond growth. To measure the TBR_{eff}, a contactless laser-based transient thermoreflectance technique was employed. A 355 nm pulsed laser is used to heat the GaN surface, inducing a rapid temperature increase, which subsequently relaxes due to heat diffusion into the layers. A 532 nm CW laser is used to monitor the surface reflectance change caused by the temperature rise as a function of time. The TBR_{eff} between GaN and diamond is then extracted by fitting the thermos-reflectance transient with a finite element thermal simulation. The laser measurement system is integrated into an optical microscope with a motorized scanning stage; this enables rapid, high spatial resolution wafer mapping. More details of the measurement can be found in references [4] and [5].

Results and Discussion

The stress in the GaN layer was characterized for a number of GaN-on-diamond wafers from different generations spanning the development stages of this technology [6]. The result is displayed in Fig. (3). In literature the stress-free E_2 peak is found to vary between 567 cm^{-1} and 567.7 cm^{-1} (grey area in Fig. 1). For comparison, GaN-on-Si and GaN-on-SiC wafers were also measured and included in the plot. Prior to year 2011, the micron-thick nitride transition layer originally from the GaN-on-Si wafer was kept between the GaN and diamond. These early wafers show a tensile stress of 0.4 - 0.5 GPa. Later wafers incorporated the removal of the nitride transition layer to lower the thermal resistance. Two diamond growth methods were then used: Hot filament (HF) CVD and microwave (MW) plasma CVD, of which the latter has become the industrial standard.

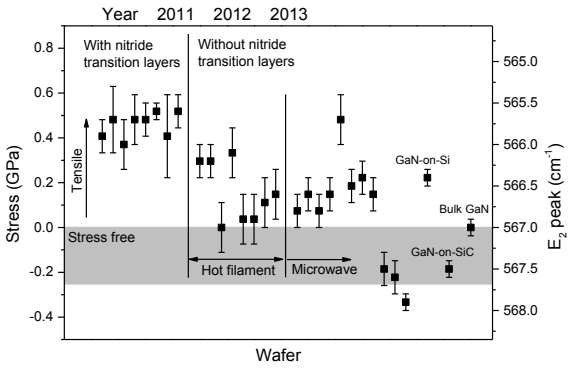

Fig. (3) The stress in the GaN layer determined by the Raman E_2 peak for various GaN-on-diamond wafers through successive generations of development. The grey area indicates E_2 peak positions in stress-free GaN from literature

From 2013 onward, the effort has been focused on optimizing the dielectric layer thickness and the diamond seeding method. The stress was alleviated and generally maintained at levels within ±0.2 GPa for both HF (after 2012) and MW growths. This highlights the role of improving the interface in stress management, which is essential for achieving crack-free, large-size GaN-on-diamond wafers with low wafer bow.

The wafer for the micro-mechanical test consisted of a ~ 0.7 μm-thick GaN, a 40 nm-thick dielectric interlayer, and a 100 μm-thick MW diamond substrate. As illustrated in Fig. (4), the whole structure was milled by focused Ga^+ ion beam to form a micro-pillar with the top GaN layer reduced to a smaller cross-sectional size than the diamond base for better loading control. Fracture occurred in the GaN layer when a load of 300 μN was reached, whereas the interface and the diamond remained undamaged. This translates to a principal stress at the GaN-diamond interface as high as 3 GPa, suggesting that the interfacial strength is greater than this value. The GaN-diamond interface is therefore considered to be stable from a mechanical point of view.

Figure (5) shows the TBR_{eff} map of a three-inch GaN-on-diamond (MW) wafer with a 37 nm-thick dielectric layer. The measurement uncertainty is approximately ±10% considering the uncertainties in the GaN layer thickness and the specific heat of GaN

used in the finite element simulation. The TBR_{eff} is reasonably homogeneous across the wafer, with a slight increase from the center towards the edge. This confirms the uniform interface quality as well as consistently robust material bonding between GaN and diamond on a wafer level. These values are broadly comparable with GaN-on-Si and GaN-on-SiC wafers, and can be further reduced by optimizing the dielectric thickness and the diamond seeding [7]. The measurement technique could also be used for wafer inspection prior to HEMT fabrication. Any anomalies at the GaN-diamond interface would be apparent in the measured thermorefectance transient, as illustrated in Fig. (5), enabling pre-screening of wafers.

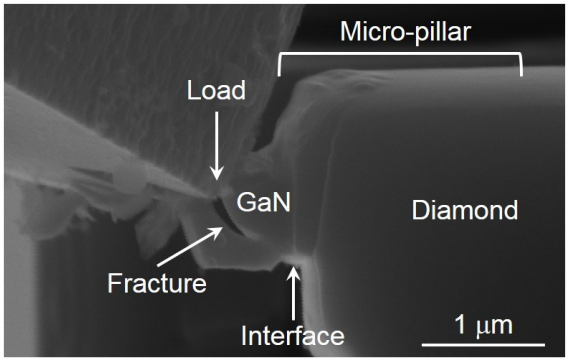

Fig. (4) *In situ* SEM graph of the micro-mechanical strength test. Fracture occurred in the GaN layer at a load of ~ 300 µN

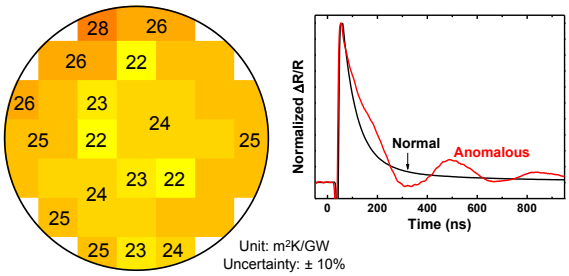

Fig. (5) Three-inch GaN-on-MW diamond wafer and its TBR_{eff} map. Representative thermoreflectance transients are shown corresponding to normal regions and a local imperfection (data from a different wafer, for illustration only), respectively

An analytical, numerical model for the two dimensional quantum well resistivity of AlGaN/GaN based high electron mobility transistors has been developed that is capable to predict accurately the effects of depletion layer thickness on the resistivity in different temperature, gate source biases and two dimensional electron gas density . Salient features of the model are incorporated of fully and partially occupied sub-bands in the interface quantum well, combined with a self-consistent solution of the Schrödinger and Poisson equations. In addition traps effects in the surface [8], interface and buffer layers, current in AlGaN barrier and three-dimensional electron gas mobility in the barrier of AlGaN and are also taking in to account. To calculate the total drain current, the both two dimensional electron gas channel (I_{2DEG}) and AlGaN barrier currents (I_{AlGaN}) have been calculated. The expression of device current can be obtained as [9]

$$I_{total} = \begin{cases} I_{AlGaN} + I_{2DEG} & for \quad d_2 < d_{AlGaN} \\ I_{2DEG} & for \quad d_2 \geq d_{AlGaN} \end{cases} \quad (1)$$

where d_{AlGaN}, d_2 are the AlGaN barrier thickness and depletion distance in gate edge near the drain side of AlGaN/GaN high electron mobility transistors respectively. So that in this model total mobility can be obtained as [10]:

$$A_1 = \frac{\mu_{2DEG} N_{2DEG}(T,m,d_2,T_{ch})}{N_{2DEG}(T,m,d_2,T_{ch}) + N_{AlGaN}} \quad (2a)$$

and

$$A_2 = \frac{\mu_{AlGaN} N_{AlGaN}}{N_{2DEG}(T,m,d_2,T_{ch}) + N_{AlGaN}} \quad (2b)$$

$$\mu_{total} = A_1 + A_2 \text{ for } d_2 < d_{AlGaN} \quad (2c)$$

or

$$\mu_{total} = \mu_{2DEG} \text{ for } d_2 \geq d_{AlGaN} \quad (2d)$$

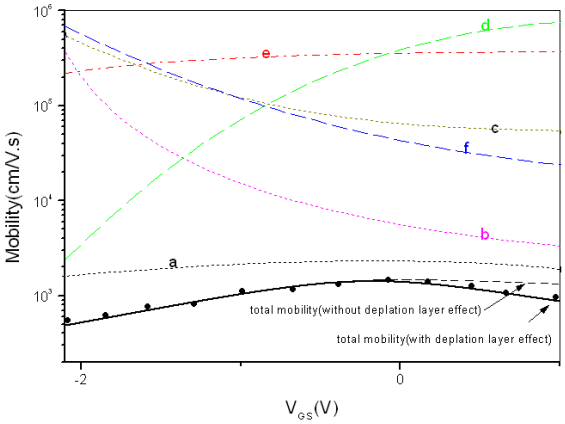

Fig. (6) Total mobility verse gate source bias at 300 K for $Al_{0.15}Ga_{0.85}N$/GaN based HEMT in comparison with existence experimental data (circles) from Ref. [4]. The different scattering mechanism in the figure labeled as (a) polar optical phonon, (b) interface roughness, (c) acoustic phonon (deformation potential and piezoelectric), (d) dislocation, (e) residual impurity and (f) alloy disorder respectively

The calculated model results are in very good agreement with existing experimental data for high electron mobility transistors device.

Conclusions

GaN-on-diamond technology for high-power transistors has seen substantial progress in recent years. The stress in the GaN layer has nearly been eliminated through optimization of the diamond seeding and growth. The GaN-diamond interface exhibits great mechanical strength, and the interfacial thermal resistance is nearly homogeneous across the wafer. The robust mechanical and thermal properties lay a crucial basis for a reliable electronic device technology.

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References

[1] D. C. Dumka, T. M. Chou, F. Faili, D. Francis, and F. Ejeckam, *IEEE Electron Lett.* 49(20), 1298 (2013).

[2] J. W. Pomeroy, M. Bernardoni, D. C. Dumka, D. M. Fanning and M. Kuball, *Appl. Phys. Lett.* 104(8), 083513 (2014).

[3] J.-M. Wagner and F. Bechstedt, *Phys. Stat. Sol. (b)* 234(3), 965 (2002).

[4] J. W. Pomeroy, R. B. Simon, H. Sun, D. Francis, F. Faili, D. J. Twitchen, and M. Kuball, *IEEE Electron Device Lett.* 35(10), 1007 (2014).

[5] H. Sun, J. W. Pomeroy, R. B. Simon, D. Francis, F. Faili, D. J. Twitchen, and M. Kuball, in *Proceedings of Compound Semiconductor Manufacturing Technology*, p. 151, Scottsdale, AZ, USA, May 2015.

[6] F. Ejeckman, D. Francis, F. Faili, D. J. Twitchen, B. Bolliger, D. Babicand, and J. Felbinger, in *Proceedings of Lester Eastman Conference on High Performance Devices*, S2-T1, Ithaca, NY, USA, August 2014.

[7] H. Sun, R. B. Simon, J. W. Pomeroy, D. Francis, F. Faili, D. J. Twitchen, and M. Kuball, *Appl. Phys. Lett.* 106(11), 111906 (2015).

[8] A. Asgari, M. Kalafi, L. Faraone, "Effect of partially occupied sub-bands on 2D electron mobility in $Al_xGa_{1-x}N$/GaN heterostrctures", *J. Appl. Phys.*, 95 (2004) 1.

[9] R. Yahyazadeh, A. Asgari, M. Kalafi, "Effect of depletion layer on negative differential conductivity in AlGaN/GaN high electron mobility transistor", *Physica E* 33 (2006) 77-82.

[10] Z. Hashempour, A. Asgari, S. Nikipar, M.R. Abolhasani, M. Kalafi, "Numerical performance evaluation of AlGaN/GaN high electron mobility transistor including gate length effects", *Physica E* 41 (2009) 1517-1521.