Electrical Properties of Oxidized Porous Silicon

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الخلاصة

في هذا البحث، تم دراسة تأثير الأكسدة الحرارية السريعة على الخصائص الكهربائية وميكانيكية التوصيل للسليكون المسامي المحضر بطريقة تشعيع الليزر أثناء عملية القشط الكهروكيميائي باستخدام ليزر ثنائي الوصلة يمتلك طول موجي 810 nm مع قدرة 2W ، عملية الأكسدة تمت باستخدام مصباح التنكستن الهالوجيني يمتلك قدرة1000W . خصائص تيار- فولتية في حالة الظلام لتركيب Al/ PS/ Si/ Alبينت تصرف مفرق هجين متجانس PS/n-Si للعينات بدون أكسدة و MIS(معدن-عازل- شبه موصل) للعينات المؤكسدة ناتج من حاجز شوتكي بعد عملية الأكسدة. من خلال دراسة الخصائص الكهربائية وجد زيادة حاجز الجهد ونسبة التقويم مع زيادة زمن الأكسدة، قيمة حاجز الجهد تغيرت من (0.65 إلى 0.72 eV) ،نسبة التقويم تغيرت من (4 الى22). المقاومية و تيار الإشباع قلت بعد عملية الأكسدة حيث قلت المقاومية من (98 إلى 65 Ω.cm) ،تيار الإشباع قل من(1.2 إلى $0.06\mu A/cm^2$).

ABSTRACT

In this research, we studying the effect of rapid thermal oxidation treatment on the electrical and conduction mechanism properties for porous silicon prepared by photo electrochemical etching by using diode laser has 810nm wavelength with power 2W. Oxidation process occurs by using tungsten halogen lamp with power 1000W. Dark I-V characteristics of Al/ PS/ Si/ Al structure shows a behavior of PS/n-Si isotype heterojunction for fresh device and a MIS (metal-insulator-semiconductor) for device after oxidation due to contribution of Al/PS schottky barrier after oxidation process. After investigated current–voltage (J-V) measurement, we found increase in barrier height and rectification ratio with increasing oxidation time, the barrier height changed (0.65 to0.72 eV), rectification ratio was varied from (4 to 22). The resistivity and saturation current density will be decreased after oxidation process where the reasistivity was decreased from ((98 to 65 Ω.cm), saturation current density was decreased from (1.2 to 0. 06 $\mu A/cm^2$).

INTRODUCTION

Since Canham [1] demonstrated visible light photoluminescence (PL) from porous silicon (PS), much effort has been focused on the possibility of producing optoelectronic devices by using this new material. SiO_2/PS systems are different in their electrical properties compare with silicon dioxide and silica [2]. Electro luminescence (EL) is also observed from schottky diodes formed form PS under forward bias [3] it is important to study the influence of recombination center surface state and electrical contacts on the OPS (oxide porous silicon)and electrical properties ,for this purpose much attention is being paid to study the electrical properties of PSi-based structure .For most of the previous work ,the rectification ratio in (J-V)curves is

interpret in terms of the existence of shottky barriers between the metal /porous silica interface [4]. *Unagami et.al*[5] believe that the metal/psi junction is not as shottky barriers but forms a non-ideal ohmic contact. The aim of this paper is to investigate the effect of oxidation time on the electrical properties like, rectification ratio, barrier height, resistivity and ideality factor on transport mechanism for porous silicon. The purpose of utilize rapid thermal oxidation is to obtain partially oxidized not fully oxidized.

MATERIALS AND METHODS

Porous silicon samples were prepares by photo electrochemical etching of (111) n-type silicon substrates with resistivity (1.5-5.5Ω.cm) in (1:1) solution of hydrofluric acid (HF) has concentration (47%) and ethanol at current density (40mA/cm^2) for (10min).The wafer has been cut out into small fragments in dimensions of (1.5×1) cm^2 ,these pieces were rinsed with ethanol to remove dirt followed by etching in dilute (10%)hydrofluoric (HF)acid to remove native oxide layer flowed by ethanol after that leave it to dry and consumed in container fully by ethanol to prevent it to oxide. The simple set–up of photo electrochemical etching process (PEC)consisted of one commercially available continues diode laser with power (2W) and (810nm) wavelength .The photo electrochemically etched area for all samples has been (0.5 cm^2). Fig. 1 depicts a schematic diagram of the photo electrochemical set-up.

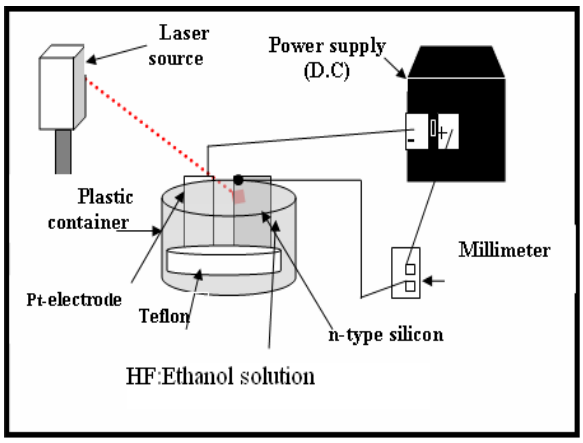

Figure - 1:Schematic digram depicts the PEC proces.

The thermal oxidation occurs at (750◦C) by using tungsten halogen lamp type (OSRAM 64575) with power (1000 W) for different oxidation times (15-150 sec) in O_2 atmosphere, to form a thin oxide layer above PS layer , fig. 2 shows the system of rapid thermal oxidation (RTO).

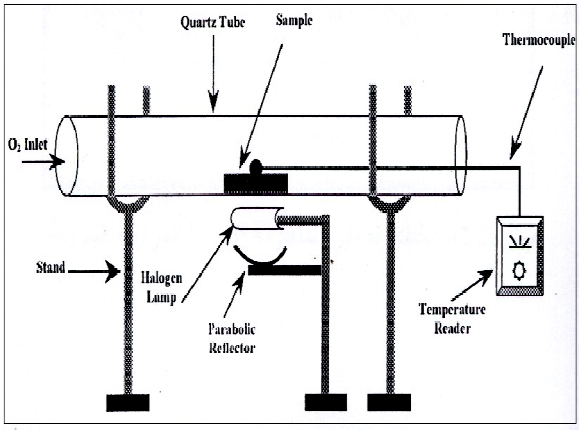

Figure - 2: Shows the manufactured system of rapid thermal oxidation.

The structure of the metal /oxide /semiconductor (MOS) photo detector is Al $_{(thin)}$/ porous silica /n-Si/AL $_{(ohmic)}$ were achieved by thermal evaporation technique. Al films was used to create an intimate backside contact the metal spot was performed on porous region to prevent direct contact between the silicon and the metal.

RESULTS AND DISCTUSIONS

Fig. 3 shows the calibration settings of the pyrometer were determined in dummy runs by calibration with thermocouple directly attached to a silicon wafer at temperature 750Ċ. Where it appear in fig.3 ,we could seen that the presence of three regions .The first region (heating region) shows the heating degree increased with irradiation time ,second region(oxidation cycle)where the temperature remains constant and rapid thermal oxidation occurred at this region ,and third region (cooling region) is obtained at moment lamp is stopping to supply the wafer by heating energy . The calibration obtained by using thermo cable with reader K-type.

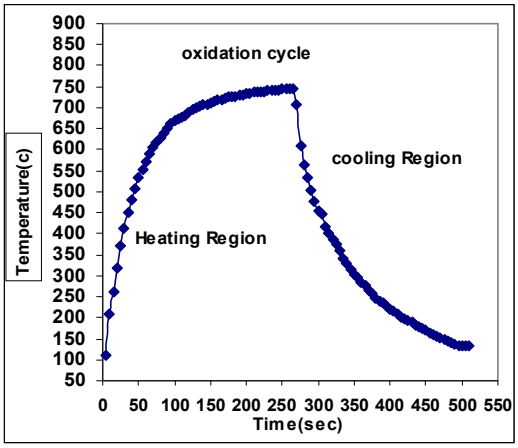

Figure -3: Shows the characteristics of RTO system.

Fig.4 shows the electrical behavior, J-V characteristics of Al/PS/Si/Al sandwich structure. Which is contains PS such as shottky diode generally is determined by depending on the characteristics of current-voltage curves [1].

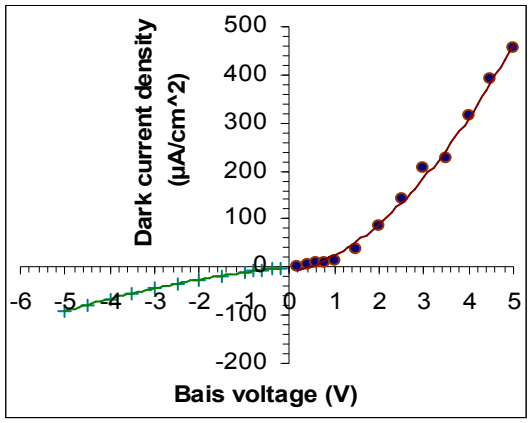

Figure -4: The J-V characteristics of as prepared PSi.

The J-V characteristics occur under dark and at room temperature of the Al/PSi/n-Si/Al sandwich structure include PS laye,shows rectifying behavior and double current saturation . We have attributed these result to silicon/porous silicon hetrojunction act as double shottky – diode [5] . Fig.5 shows J-V characteristics for PS before and after oxidation process we can observed that the reverse current would be decreased and forward current increased rather than as prepared in fig.4 which means that the rectifying behavior increased after oxidation due to the heterojunction potential barrier at the oxide /PSi interface that attributed to the quantum confinement in silicon nano crystallites [6].

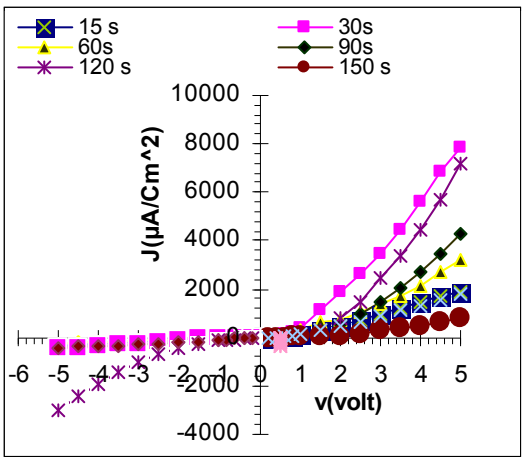

Figure -5: The J-V characteristics of the junction.

Fig .6 shows the rectifying characteristics obtained at 5-volt.The rectification ratio mean the ratio between forward current to the reverse current, it is for as prepared sample was equal to 4.1, with increasing oxidation time the rectification ratio increases and reach to optimum value about 22 at oxidation time (30sec).

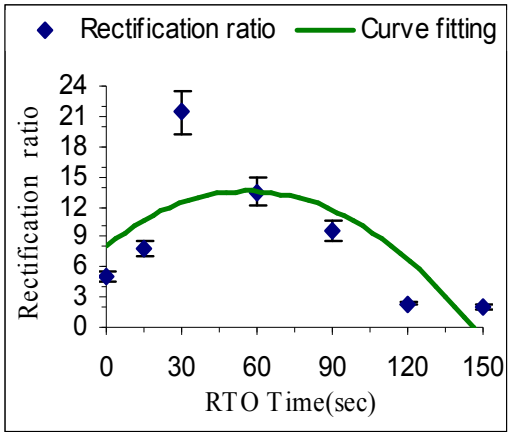

Figure -6: Shows rectification ratio versus oxidation times.

That increased in rectification ratio after oxidation process is attributed to the formation of a thin oxide layer between AL / metal and PS layer[7] and formation of an isotope heteojunction ,after that time the rectification ratio will be decreased that due to the defect formed by the sympathize silicon-oxygen structure in a very thin oxide layer and they would act as tunneling center, for oxidation time is longer than (30 sec) the oxide layer is thicker the tunneling probability of photo carriers and the thermal generated carriers through the oxide layer are reduced and hence the dark current to be reduced [8].The oxide thickness is estimated by using equation for high resistivity n-type silicon wafer[9]:

$$R_0 = 1.8 \times 10^5 \exp\left[\frac{-1.21}{kT}\right] \cdots (1)$$

where R◦ is the oxidation rate Å/s ,1.21eV is the activation energy required to diffuse oxygen inter silicon for rapid thermal oxidation and it is equal to 2 eV for Deal –Grove model (classical dry oxidation) ,the oxide thickness which obtain by theoretical equation (1) is illustrated in fig. 7.

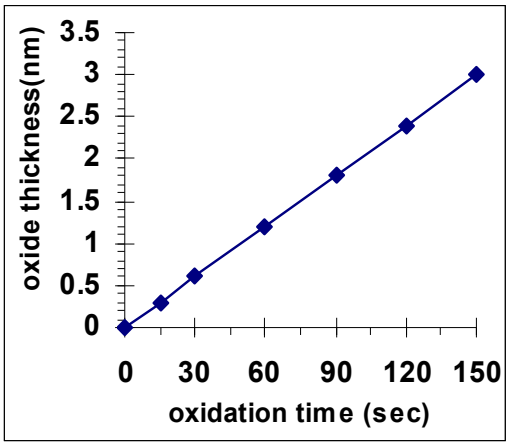

Figure -7: The oxide thickness at deferent oxidation time

The typical of the measured J-V is very similar to shottky diode characteristics and may analyze by using the following equation which described by [10]:

$$J = J_s [\exp \left[\frac{qv}{nkT} \right] - 1] \cdots \quad (2)$$

Where *Js* ($\mu A/cm^2$) is the saturation current density obtained from semi-log forward bias, *k* (J/K) is Boltzman constant, *T* (K) is room temperature, *q*(C) electron charge, and *n* ideality factor is given by the following equation [10]:

$$n = \frac{q}{kT} \frac{\partial v}{\partial \ln J} \cdots \quad (3)$$

The ideality factor defines as approach of device from ideality charecterstics, fig.8 shows the changing in ideality factor with oxidation time, we can observed of decreasing ideality factor with increasing oxidation time where it changed from 16 to 2.7 at oxidation time 30 sec .That decreasing due to decrease density of state after oxidation lead to decrease ideality factor according to relation[11]:

$$n = 1 - \frac{\delta \varepsilon_s}{W \varepsilon_i} + \frac{\delta q D_s}{\varepsilon_i} \ldots\ldots (4)$$

where *Ds* in (cm^{-2} eV^{-1})is the density of state available to store charge in the inter phase layer at the semiconductor space charge region, *W* is the width of the semiconductor space charge region, ε_i, ε_s are the dielectric constant for the inter phase and semiconductor regions, respectively ,where ε_i=3.9, and ε_s=11.9 ,and□□□ is the thickness of

the interface layer,with increasing oxidation time larger than 30 sec we can observed that the ideality factor is come back to increase that due to the presence of surface channel in our diodes[12],see Table.1.

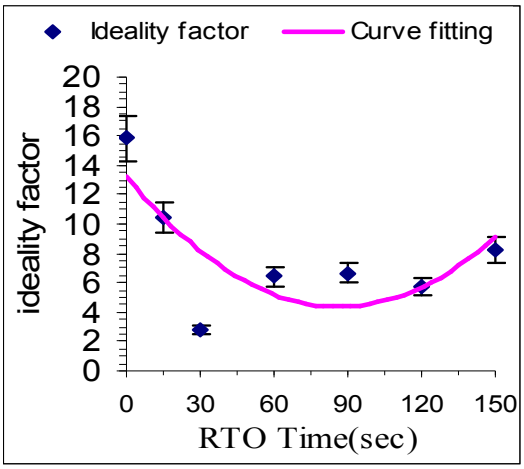

Figure-8: The ideality factor for as prepared and at different oxidation times.

Table -1: Shows the electrical values with different oxidation times.

Oxidation time(sec)	Rectification ratio	Saturation current ($\mu A/cm^2$)	Ideality factor	Barrier Height (eV)
as prepared	4.1	1.2	16	0.65
15	7.4	1.3	11	0.648
30	22	0.06	2.7	0.728
60	13	1	6.4	0.655
90	8.9	1.2	6.66	0.650
120	2	1.4	6	0.646
150	1.8	1.6	8	0.643

We can calculate resistivity for PSi after and before thermal oxidation from J-V curve, fig.9 shows behavior of resistivity with oxidation time.

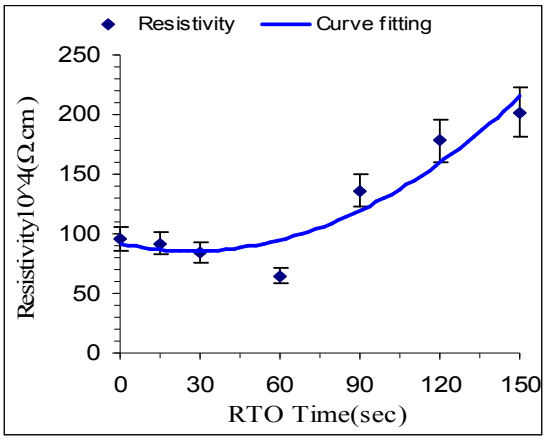

Figure-9: The resistivity with oxidation time.

From fig.9 we can notice that at oxidation time(15-60)sec the resistivity will be decrease from (98 to 65)Ω.cm that is due to the PS layer have a very large effective surface area and has a large mount from dangling bonds after oxidation the dangling bonds is replaced by pure oxygen bonds that increasing conductivity which lead to decreasing resistivity [6], with increasing oxidation time the resistivity come back to increase and reached to 212 Ω.cm at oxidation time 150 sec that increasing due to increase porous layer depth with increasing oxidation time [13] which lead to increase resistance according to relations[12]:

$$R = \rho \frac{A}{d} \quad .....(5)$$

Where R (Ω) resistance, ρ (Ω.cm) resistivity, A (cm^2) sample area, d (cm) porous layer thickness.

The barrier height was founded to increase with oxidation time and have maximum value at oxidation time (30sec) about (0.728 eV) we can calculate the barrier height from saturation current density (Js (A/cm^2)) [12].

$$J_s = A^{**}T^2 \exp\left[\frac{q\phi_{Bn}}{kT}\right] \quad .....(5)$$

Where A^{**} is the effective Richardson which equal to 120($A/K^2.cm^2$) for n-type, from equation the barrier height is given by following equation [12]:

$$\Phi_{Bn} = \frac{k_B T}{q} \ln\left(\frac{A^{**}T^2}{J_s}\right) \quad .....(6)$$

Fig.10 shows the increasing of barrier height with increasing oxidation time, where it is varied from (0.65 to 0.728) eV at oxidation time 30 sec.

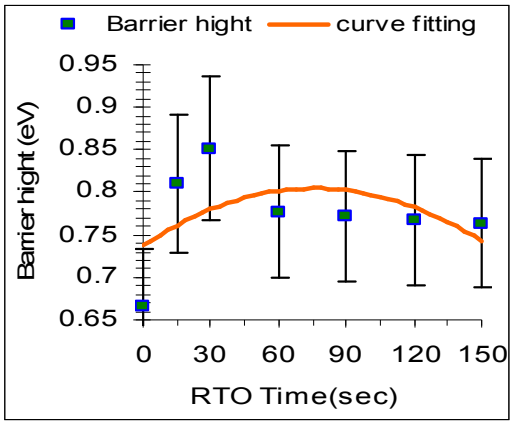

Figure-10: The barrier height with oxidation time.

The increase in barrier height with increasing oxidation time is attributed to:

1-Barrier height for PS depending on the barrier height of the M/PSi/n-Si/M,the PS/c-Si interface have pinning which acts as a defect in the interface leading to increase saturation current [8-13]after oxidation the interface layer become clean because thermal oxidation replace unstable hydrogen and oxygen by pure oxide layer that lead to decrease saturation current subsequently increasing barrier height because the barrier height inversely proportion with saturation current according to relation (6)[8] . Table .1 shows the values of barrier height according to the value of saturation current density (Js) with different oxidation time.
2-The increasing barrier height is attributed to formation of MIS structure at Al/PSi/Si/ Al by producing an oxide interfacial layer after RTO process the oxide layer lead to add new potential height to the barrier height equation and it will be given by the following equation [12]:
The equation (7) can give by [12]:

$$\phi_T = \frac{kT}{q} Ln \frac{A^* T^2}{J_S} + \frac{kT}{q} \chi^{1/2} \delta \ldots\ldots (7)$$

$$\phi_T = \phi_{Bn} + \frac{kT}{q} \chi^{1/2} \delta \ldots\ldots (8)$$

where χ (eV) is average barrier height, δ (Å)the oxide thickness, equation (8) represent the effective barrier height for metal /oxide/semiconductor contact. In fig.10 we can seen that decreasing barrier height with increasing oxidation time that due to increase saturation current density also with increasing oxide thickness the oxide charge appear like positive charge working as pinhole effort to capture the transmition carrier which caused to decrease barrier height in the contacts region[9-14].

SiO_2/PS layer in this study formed by using rapid thermal oxidation process in O_2 atmosphere pressure, ideality factor, rectification ratio ,barrier height and resistivity were measured at different oxidation time (15-150) sec at temperature 750 Ċ ,we observed the barrier the rectification ration was 4.1 before oxidation will be 22 after 30 sec oxidation time ,barrier height value was (0.65eV) will be(0.72 eV) at oxidation time 30 sec ,the ideality factor after oxidation was 16 will be 2.7 at 30 sec of oxidation time after this time the barrier height and rectification ratio begin to decrease due to increase oxide layer thickness working to consume column by growth within PS layer caused to increase energy gap that lead PS behavior like insulator .

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